

Starload Schematics

Skylake-U

2016-02-18

REV : A00

www.teknisi-indonesia.com

DY : None Installed

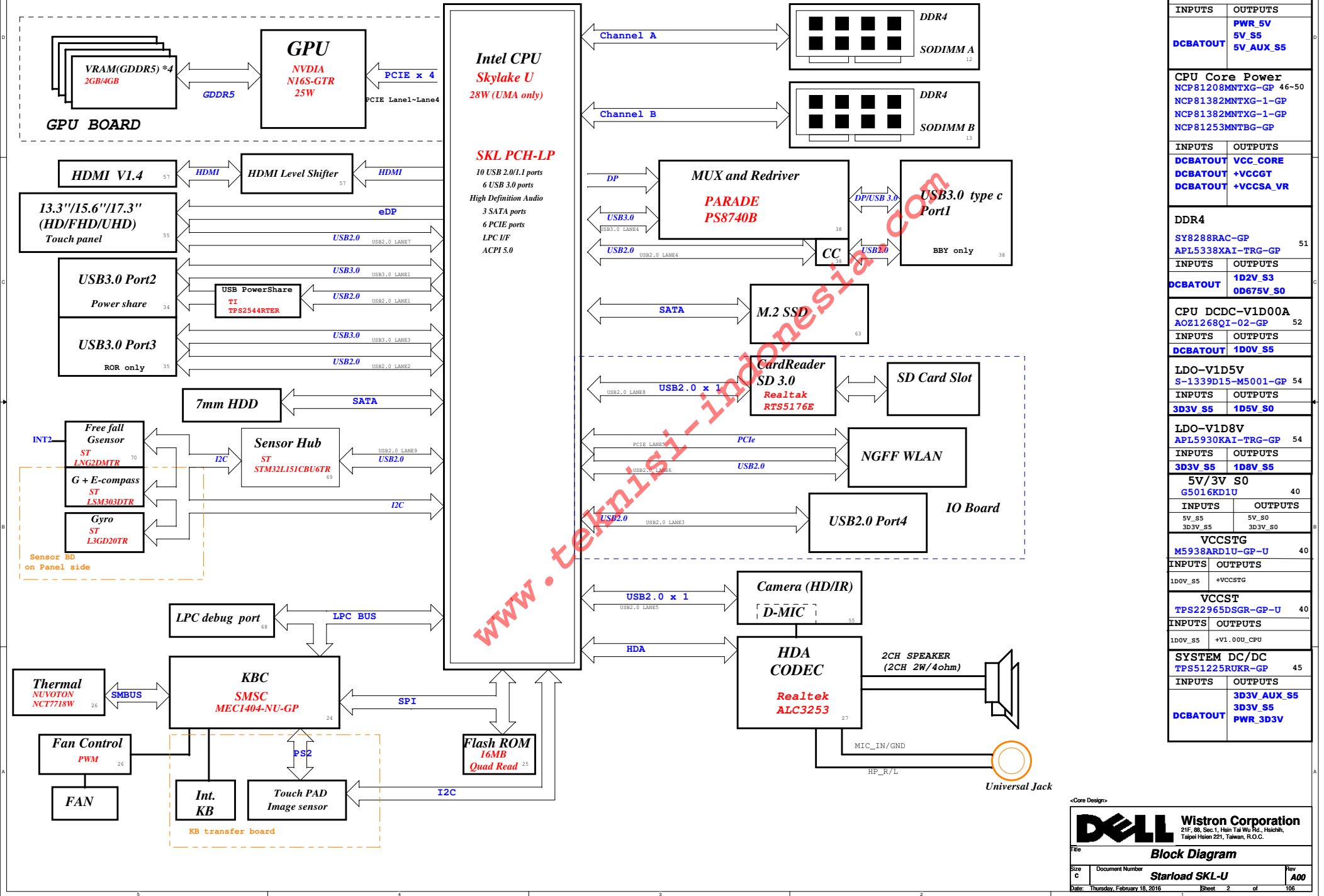
UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Variant Name>		
DELL Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Cover Page		
Size A3	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2016	Sheet 1	of 106

Project code: 4PD07S010001
PCB P/N: 15264
Revision: A00

Star lord SKL-U Block Diagram




CHARGER		44
ISL95521HRZ-T		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
SY8288CRAC-GP		
INPUTS	OUTPUTS	
DCBATOUT	PWR_5V 5V_S5 5V_AUX_S5	
CPU Core Power		46~50
NCP81208MNTXG-GP		
NCP81382MNTXG-1-GP		
NCP81382MNTXG-1-GP		
NCP81253MNTBG-GP		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DCBATOUT	+VCCGT	
DCBATOUT	+VCCSA_VR	
DDR4		51
SY8288RAC-GP		
APL5338XAI-TRG-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D2V_S3 0D675V_S0	
CPU DCDC-V1D00A		52
AOZ1268Q1-02-GP		
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	
LDO-V1D5V		54
S-1339D15-M5001-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
LDO-V1D8V		54
APL5930KAI-TRG-GP		
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	
5V/3V_S0		40
G5016KD1U		
INPUTS	OUTPUTS	
5V_S5	5V_S0	
3D3V_S5	3D3V_S0	
VCCSTG		40
M5938ARD1U-GP-U		
INPUTS	OUTPUTS	
1D0V_S5	+VCCSTG	
VCCST		40
TPS22965DSGR-GP-U		
INPUTS	OUTPUTS	
1D0V_S5	+V1.000_CPU	
SYSTEM DC/DC		45
TPS51225RUKR-GP		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 3D3V_S5 PWR_3D3V	

Main Func = CPU

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A3

Document Number

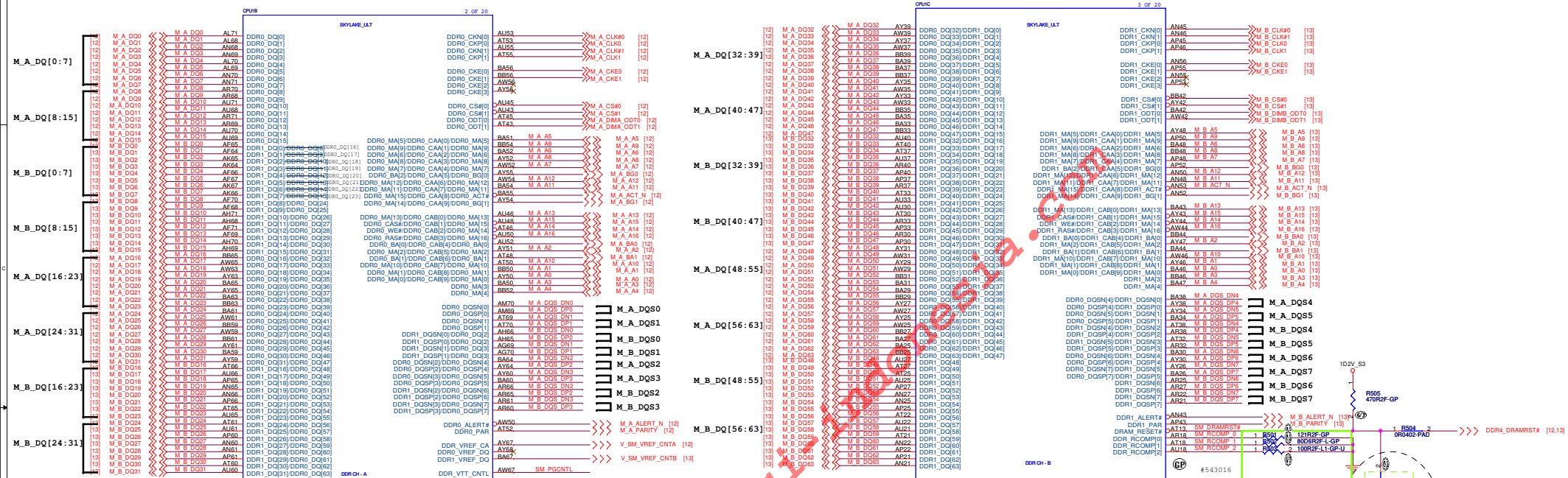
Starload SKL-U

Rev

A00

Date: Thursday, February 18, 2016

Sheet 3 of 106



DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

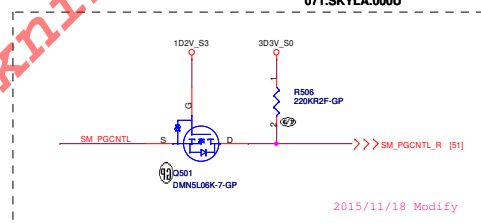
PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	DRAMs	DDR0_ODT[0] connected to DIMM ODT	1,2	Topology connection
			One ODT per x32 DRAM PKG		
SKL-U	LPDDR3 Memory Down	DRAMs	DDR0_ODT[1:0] connected to DIMM ODT	1,2	Topology connection
			One ODT per x32 DRAM PKG		
DDR3L Memory Down	DRAMs	DRAMs	DDR0_ODT[1:0] connected to DIMM ODT	3,4	Topology connection
			One ODT per x32 DRAM PKG		
DDR3L SO-DIMM	DIMM	DIMM	DDR0_ODT[1:0] connected to DIMM ODT	1,3	Topology connection
			One ODT per x32 DRAM PKG		
DDR3L Head Memory Down	DIMM	DIMM	DDR0_ODT[1:0] connected to DIMM ODT	3,4	Topology connection
			One ODT per x32 DRAM PKG		
DDR4 Memory Down	DRAMs	DRAMs	DDR0_ODT[1:0] connected to DIMM ODT	1,2	Topology connection
			One ODT per x32 DRAM PKG		
DDR4 SO-DIMM	DIMM	DIMM	DDR0_ODT[1:0] connected to DIMM ODT	1,3	Topology connection
			One ODT per x32 DRAM PKG		

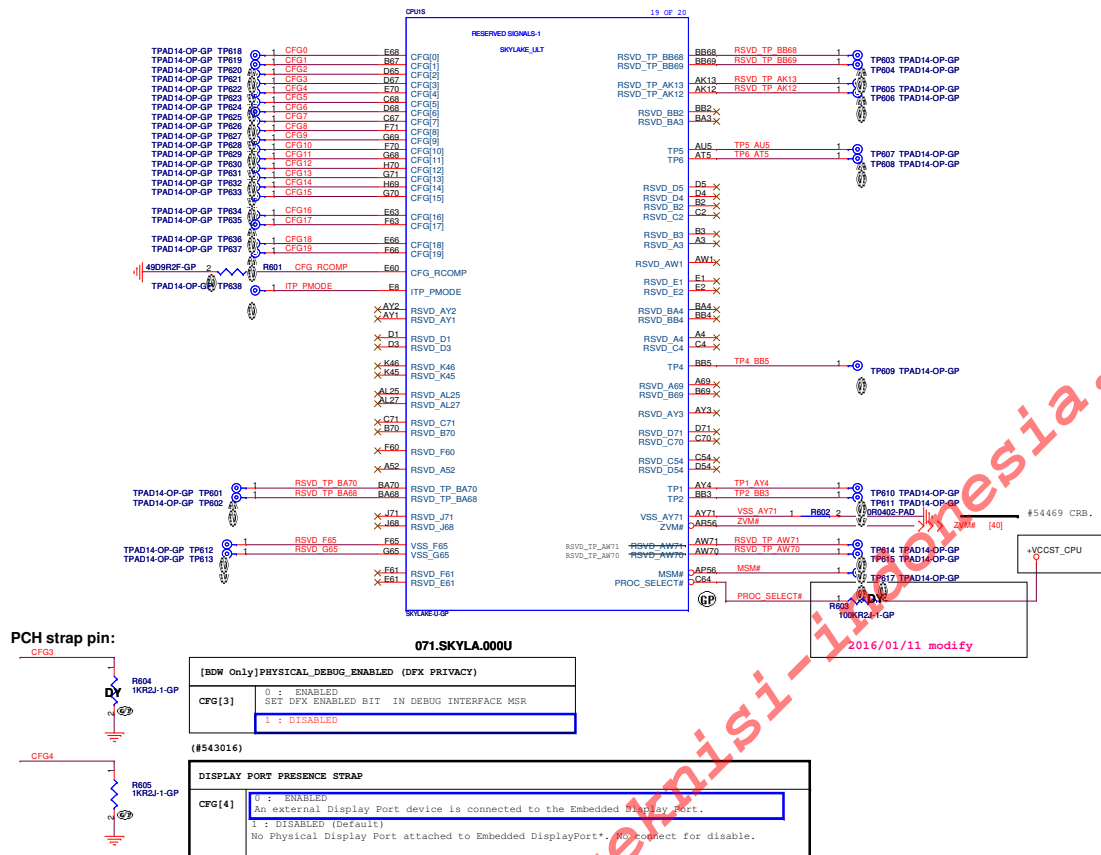
Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (VDFP - SKL-Y LPDDR3, VDFP - SKL-U LPDDR3, VDFP - SKL-Y LPDDR3, VDFP - SKL-U LPDDR3).
2. DDR0_ODT signal is used for ODT. If not used, it should be connected to GND. In both cases, when a Bank receives write command it enables R/W bit (set by BIOS after power training). Otherwise ODT pins R/W bit (high-impedance).
3. These guidelines are related to DDR3L supported memory down topologies only. 2R x16 DDP single side, 2R x16 DDP dual side and 2R x8 dual side.



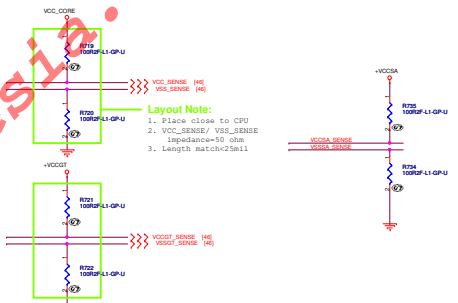
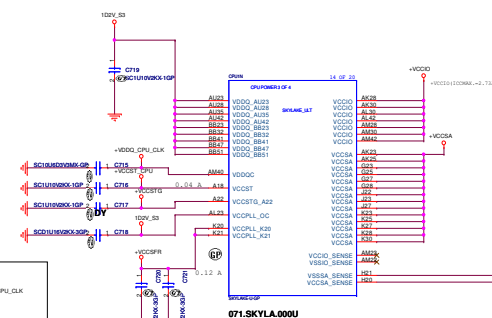
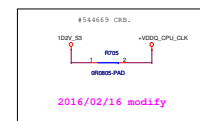
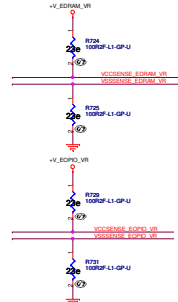
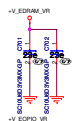
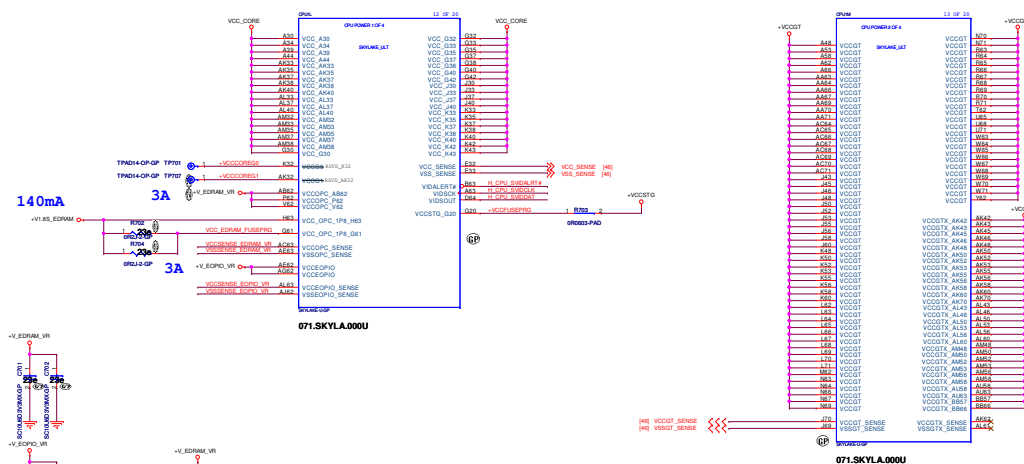
Design Guidelines:
SM-RCOMP keep routing length less than 500 mils.

Layout Note:

close to CPU



<Core Design>



SVID DATA



SVID CLOCK

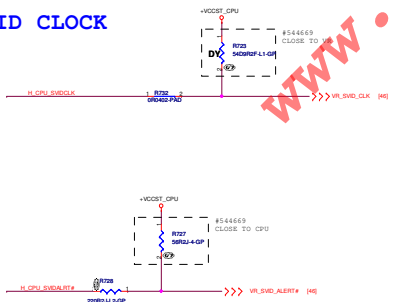


Figure 10-7. Routing Illustration for SVID Topology

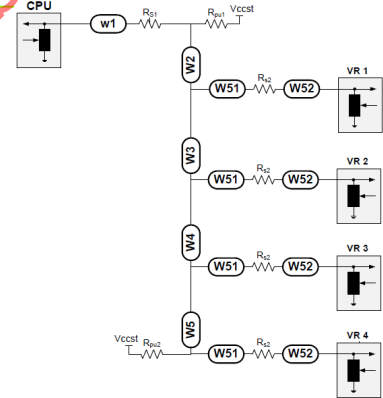
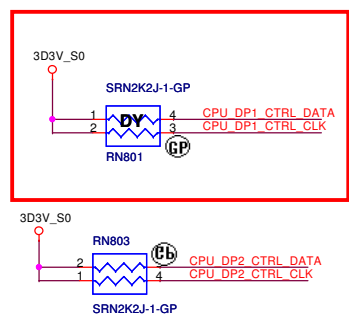


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W1 [inches]	W2 [inches]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	R _{DS(on)} [Ω]	V _{CE(sat)} [V]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT							56	Empty	220	0	

Dummy, Vendor suggest
20141117

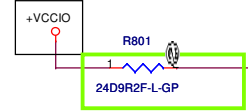


HDMI

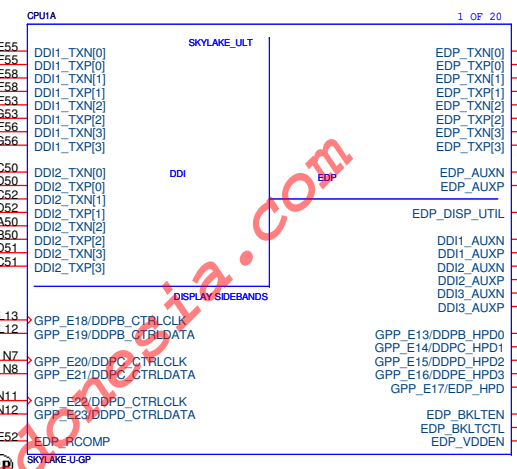
DP and DP to VGA

HDMI

Check



- [57] HDMI_DATA2#
- [57] HDMI_DATA2
- [57] HDMI_DATA1#
- [57] HDMI_DATA1
- [57] HDMI_DATA0#
- [57] HDMI_DATA0
- [57] HDMI_CLK#
- [57] HDMI_CLK
- [38] PCH_DPC_N0
- [38] PCH_DPC_P0
- [38] PCH_DPC_N1
- [38] PCH_DPC_P1
- [38] PCH_DPC_N2
- [38] PCH_DPC_P2
- [38] PCH_DPC_N3
- [38] PCH_DPC_P3



- C47 EDP_TX0_DN [55]
- C46 EDP_TX0_DP [55]
- D46 EDP_TX1_DN [55]
- C45 EDP_TX1_DP [55]
- A45 EDP_TX2_DN [55]
- B45 EDP_TX2_DP [55]
- A47 EDP_TX3_DN [55]
- B47 EDP_TX3_DP [55]
- E45 EDP_AUX_DN [55]
- F45 EDP_AUX_DP [55]
- B52 EDP_DISP_UTIL_1
- TP801 TPAD14-OP-GP
- G50 DD11_AUXN
- F50 DD11_AUXP
- F48 DD12_AUXN
- F48 DD12_AUXP
- G46 DD13_AUXN
- F46 DD13_AUXP
- L9 CPU_DP2_HPD
- L7 CPU_DP1_HPD [57]
- L6 SIO_EXT_SMI# [24]
- N9 EDP_HPD [55]
- L10
- B12 L_BKLT_EN [24]
- B11 L_BKLT_CTRL [55]
- U13 EDP_VDD_EN [55]

071.SKYLA.000U
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

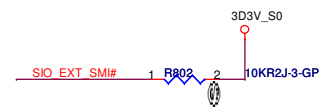
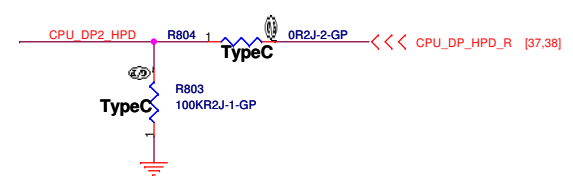
(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω \pm 1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k \pm 5% resistor	NC

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω resistor.



Main Func = CPU

(Blanking)

www.teknisi-indonesia.com

(#543016 PDS)

CORE

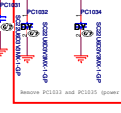
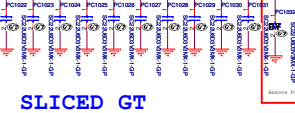
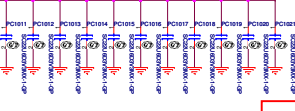
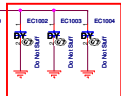
20140814 DAVID

U-line 23a 28W
IccMax current-10ms max = 34 A

220 0603 x 35 (5 DT)



SMT reserve , 20141118

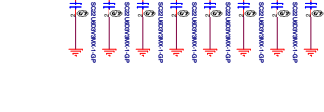
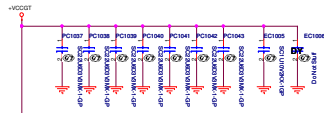


Remove PC1020 and EC1005 (Power team request)

SLICED GT

U-line 23a 28W
IccMax current-10ms max[A] = 67 A

220 0603 x35 (5 DT)



2015/10/16 modify (Power team request)

VCCSA

220 0603 x13 (5 DT)



Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at backside side near to VR output
VCCGT Power Plane at VR output	2x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCGTx Power Plane at VR output	1x 220uF (04.5mD ESR)	Placed at primary side near to VR output
VCCIO Power Plane at VR output	2x 47uF 0805	Additional components needed when supporting 23a
VCCSA Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

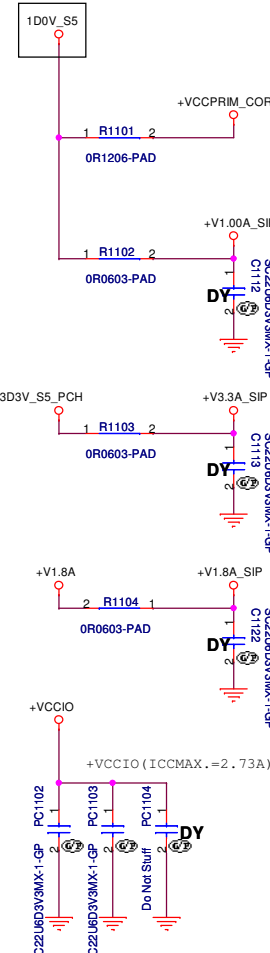
Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 220uF 0805		Place on secondary side, underneath the package
VCC	7x 10uF 0402		
VCC	15x 1uF 0201		
VCC		8x 47uF 0805 (6.3V)	Place as close to the package as possible
VCC		8x 10uF 0402	
VCCGT	10x 10uF 0402		Place on secondary side, underneath the package
VCCGT		12x 1uF 0201	
VCCGT		3x 47uF 0805 (6.3V)	Place as close to the package as possible
VCCGT		7x 22uF 0603	
VCCGT		3x 47uF 0805	Place as close to the package as possible
VCCGT		5x 22uF 0603	Additional components needed when supporting 23a
VCCGTx	8x 10uF 0402		Place on secondary side, underneath the package
VCCGTx		8x 22uF 0603	Only needed when supporting 23a
VCCSA	7x 10uF 0402		Place on secondary side, underneath the package
VCCSA		7x 1uF 0201	
VCCSA		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCIO		4x 1uF 0201	
VDDQ	2x 10uF 0402		Place as close to the package as possible
VDDQ		4x 1uF 0201	Place on secondary side, underneath the package
VDDQ		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL	1x 1uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

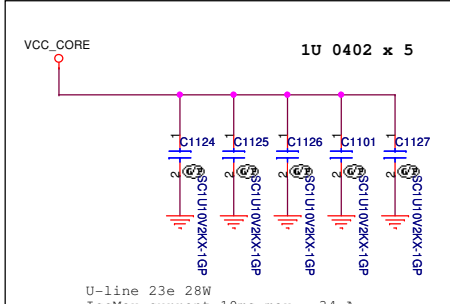
Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package
VCCSTG			Placeholder only
VCCSTG	2x 10uF 0402		Place on secondary side, underneath the package
VCCSTG	1x 10uF 0402		Place on secondary side, underneath the package
VCCSTG	6x 1uF 0201		Place on secondary side, underneath the package

Main Func = CPU

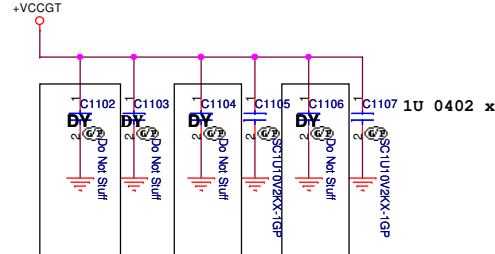
PCH DERIVED RAILS



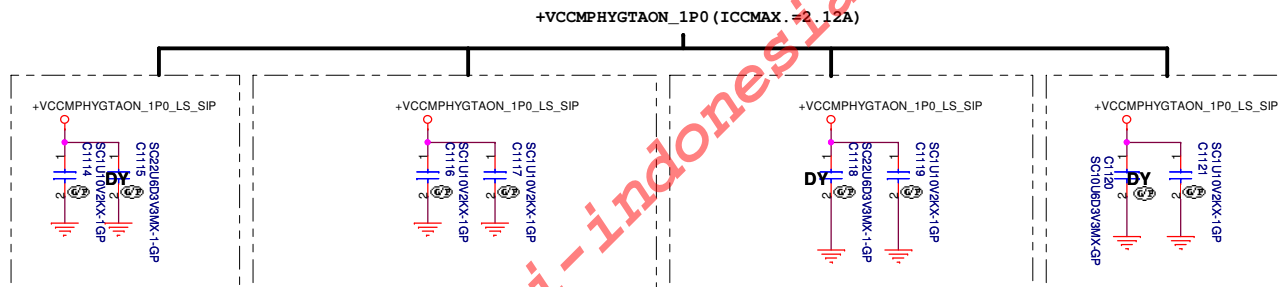
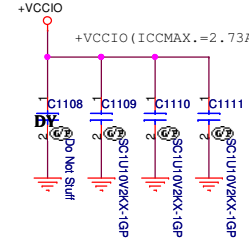
Size:0805 change to 0603
20141117



UNSLICED GT



VCCIO



Lavout Note:

1uF:

C1174 near N15

C1180 near K15

C1173 near AF20

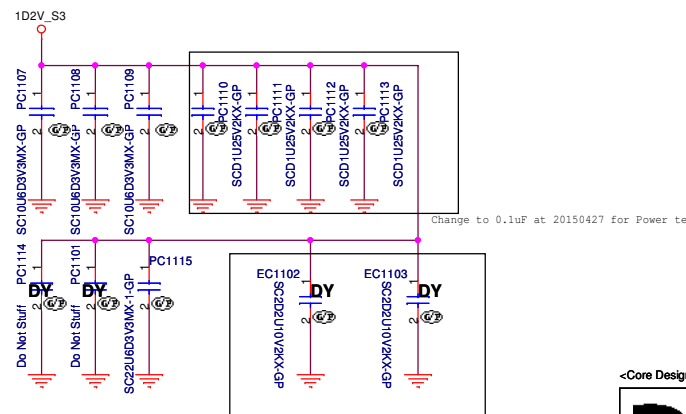
C1172 near N18

C1175 near AB19

220F :

C1182

10UF : 221F



RF request 2016/01/12 modify

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (Power CAP2)

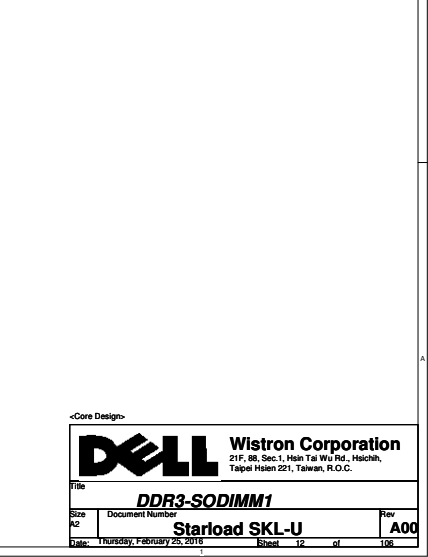
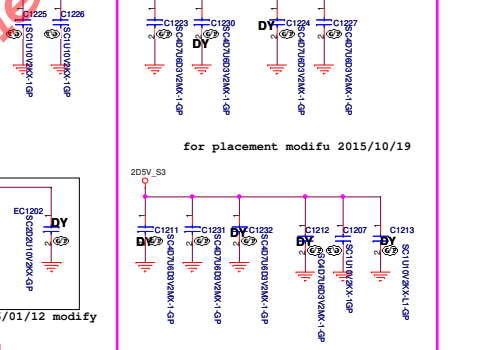
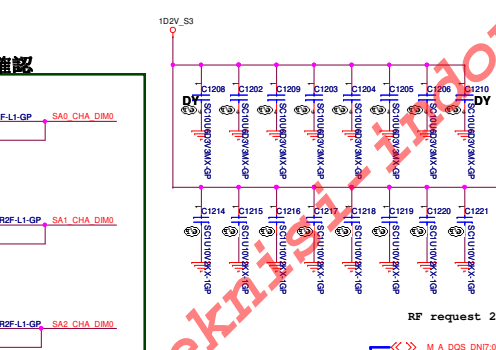
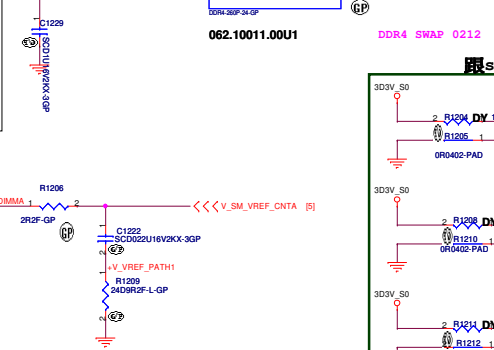
Size

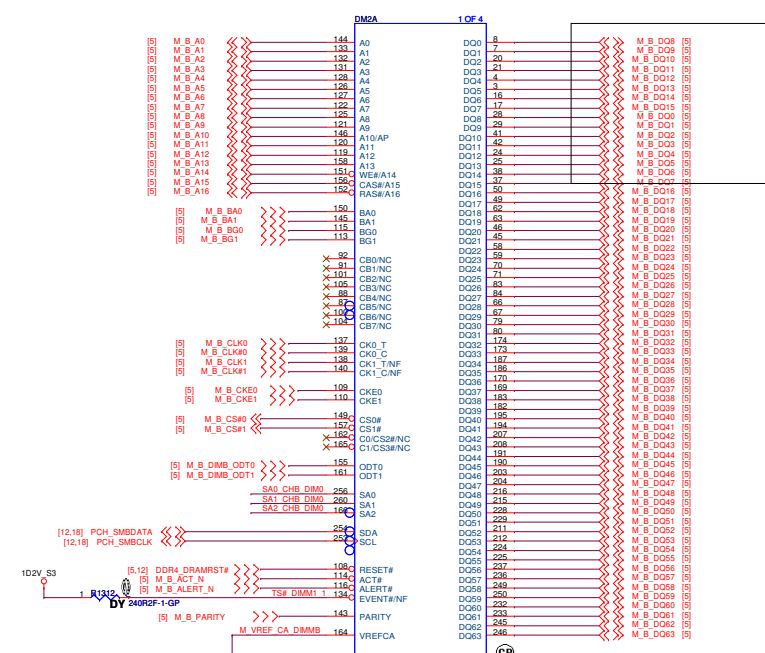
Document Number

Starload SKL-U

Date: Thursday, February 18, 2016

Sheet 11 of 106





(Blanking)

www.teknisi-indonesia.com

<Core Design>


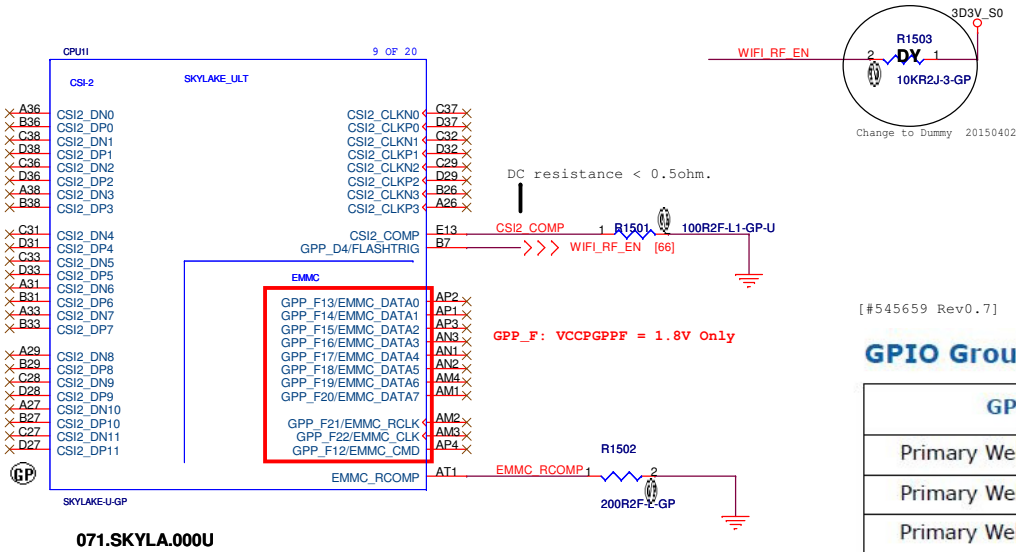
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)_SODIMM _SODIMM4		
Size A4	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2016		Sheet 14 of 106

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSENT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.



[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU_(CS-2/EMMC)

Size

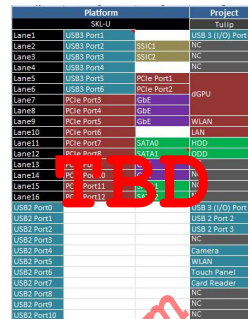
Document Number

Starload SKL-U

Rev

Date: Thursday, February 25, 2016

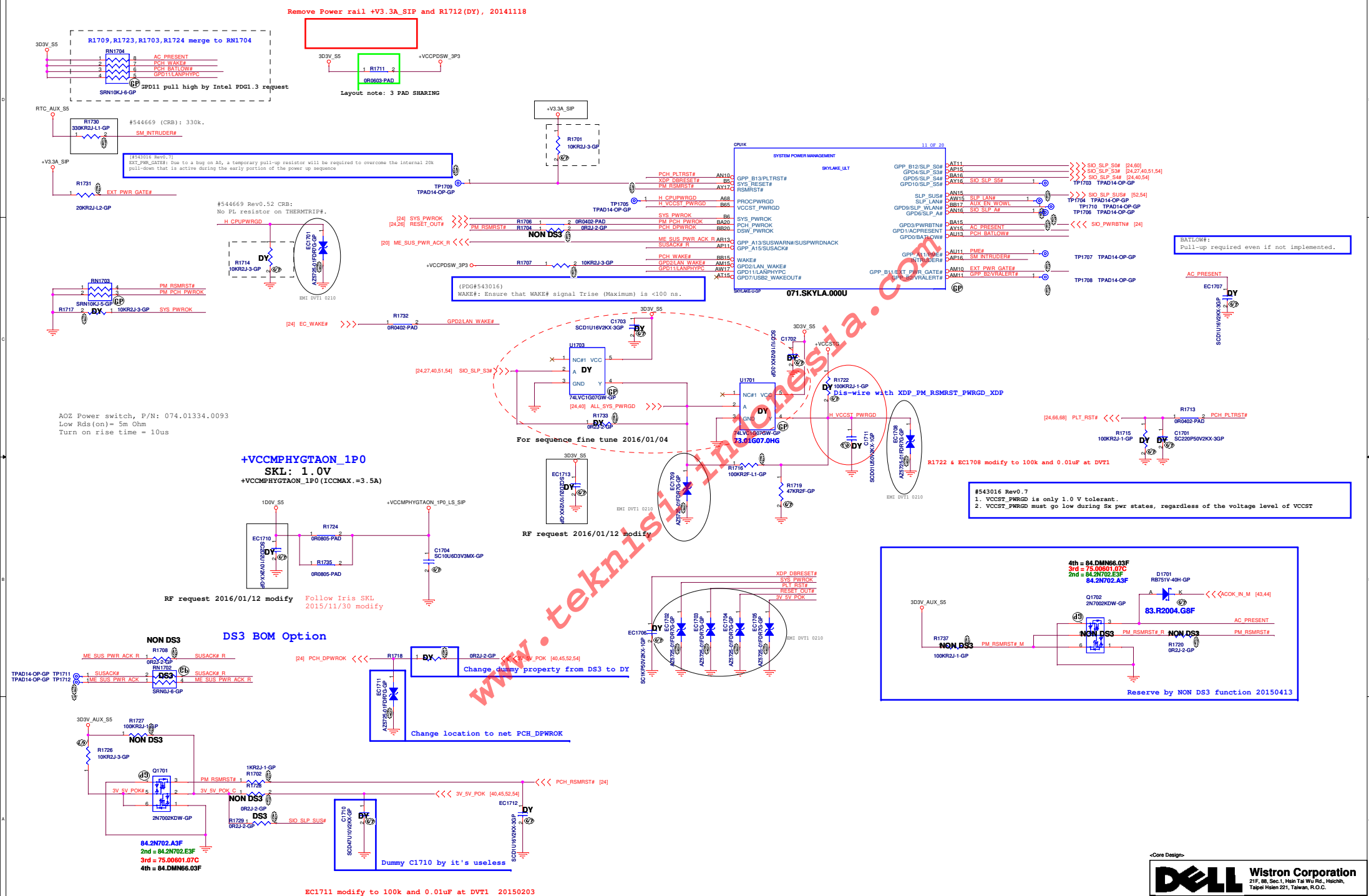
Sheet 15 of 106



SKL	Max Dev ice (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MB/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

SKL	PCIe Link Config	PCI Express® Lanes											
		1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1			Port5				Port9				
	2x2	Port1	Port3		Port5		Port7		Port9		Port11		
	1x2 + 2x1	Port1	Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12	
	2x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
		Port1			Port5								
Y	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1	Port3	Port4	Port5		Port7	Port8					
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

[illegible]

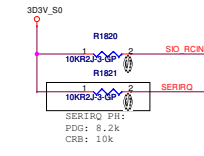
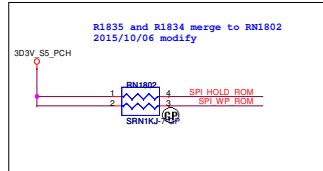


PCH strap pin:

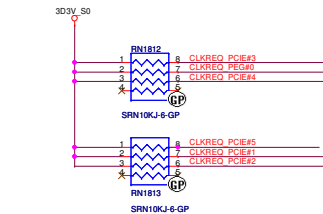
eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT#/ GPP_CS	This signal has a weak internal pull-down. 0 = LPC is selected for EC. 1 = eSPI is selected for EC. This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	SPI0_MOSI
0 = ENABLED 1 = DISABLED WEAK INTERNAL PU	This signal has a weak internal pull-up.



PCIN#:
Frequency to Avoid: 33 Mhz



WLAN

[66] CLK_PCIE_VGA#
[66] CLK_PCIE_VGA
[66] SCRCCLKREQ#0

[66] PEG_CLK1_CPU#
[66] PEG_CLK1_CPU#
[66] CLKREQ_PCIE#1

[66] CLKREQ_PCIE#2

[66] CLKREQ_PCIE#3

[66] CLKREQ_PCIE#4

[66] CLKREQ_PCIE#5

[66] CLKREQ_PCIE#6

[66] CLKREQ_PCIE#7

[66] CLKREQ_PCIE#8

[66] CLKREQ_PCIE#9

[66] CLKREQ_PCIE#10

[66] CLKREQ_PCIE#11

[66] CLKREQ_PCIE#12

[66] CLKREQ_PCIE#13

[66] CLKREQ_PCIE#14

[66] CLKREQ_PCIE#15

[66] CLKREQ_PCIE#16

[66] CLKREQ_PCIE#17

[66] CLKREQ_PCIE#18

[66] CLKREQ_PCIE#19

[66] CLKREQ_PCIE#20

[66] CLKREQ_PCIE#21

[66] CLKREQ_PCIE#22

[66] CLKREQ_PCIE#23

[66] CLKREQ_PCIE#24

[66] CLKREQ_PCIE#25

[66] CLKREQ_PCIE#26

[66] CLKREQ_PCIE#27

[66] CLKREQ_PCIE#28

[66] CLKREQ_PCIE#29

[66] CLKREQ_PCIE#30

[66] CLKREQ_PCIE#31

[66] CLKREQ_PCIE#32

[66] CLKREQ_PCIE#33

[66] CLKREQ_PCIE#34

[66] CLKREQ_PCIE#35

[66] CLKREQ_PCIE#36

[66] CLKREQ_PCIE#37

[66] CLKREQ_PCIE#38

[66] CLKREQ_PCIE#39

[66] CLKREQ_PCIE#40

[66] CLKREQ_PCIE#41

[66] CLKREQ_PCIE#42

[66] CLKREQ_PCIE#43

[66] CLKREQ_PCIE#44

[66] CLKREQ_PCIE#45

[66] CLKREQ_PCIE#46

[66] CLKREQ_PCIE#47

[66] CLKREQ_PCIE#48

[66] CLKREQ_PCIE#49

[66] CLKREQ_PCIE#50

[66] CLKREQ_PCIE#51

[66] CLKREQ_PCIE#52

[66] CLKREQ_PCIE#53

[66] CLKREQ_PCIE#54

[66] CLKREQ_PCIE#55

[66] CLKREQ_PCIE#56

[66] CLKREQ_PCIE#57

[66] CLKREQ_PCIE#58

[66] CLKREQ_PCIE#59

[66] CLKREQ_PCIE#60

[66] CLKREQ_PCIE#61

[66] CLKREQ_PCIE#62

[66] CLKREQ_PCIE#63

[66] CLKREQ_PCIE#64

[66] CLKREQ_PCIE#65

[66] CLKREQ_PCIE#66

[66] CLKREQ_PCIE#67

[66] CLKREQ_PCIE#68

[66] CLKREQ_PCIE#69

[66] CLKREQ_PCIE#70

[66] CLKREQ_PCIE#71

[66] CLKREQ_PCIE#72

[66] CLKREQ_PCIE#73

[66] CLKREQ_PCIE#74

[66] CLKREQ_PCIE#75

[66] CLKREQ_PCIE#76

[66] CLKREQ_PCIE#77

[66] CLKREQ_PCIE#78

[66] CLKREQ_PCIE#79

[66] CLKREQ_PCIE#80

[66] CLKREQ_PCIE#81

[66] CLKREQ_PCIE#82

[66] CLKREQ_PCIE#83

[66] CLKREQ_PCIE#84

[66] CLKREQ_PCIE#85

[66] CLKREQ_PCIE#86

[66] CLKREQ_PCIE#87

[66] CLKREQ_PCIE#88

[66] CLKREQ_PCIE#89

[66] CLKREQ_PCIE#90

[66] CLKREQ_PCIE#91

[66] CLKREQ_PCIE#92

[66] CLKREQ_PCIE#93

[66] CLKREQ_PCIE#94

[66] CLKREQ_PCIE#95

[66] CLKREQ_PCIE#96

[66] CLKREQ_PCIE#97

[66] CLKREQ_PCIE#98

[66] CLKREQ_PCIE#99

[66] CLKREQ_PCIE#100

[66] CLKREQ_PCIE#101

[66] CLKREQ_PCIE#102

[66] CLKREQ_PCIE#103

[66] CLKREQ_PCIE#104

[66] CLKREQ_PCIE#105

[66] CLKREQ_PCIE#106

[66] CLKREQ_PCIE#107

[66] CLKREQ_PCIE#108

[66] CLKREQ_PCIE#109

[66] CLKREQ_PCIE#110

[66] CLKREQ_PCIE#111

[66] CLKREQ_PCIE#112

[66] CLKREQ_PCIE#113

[66] CLKREQ_PCIE#114

[66] CLKREQ_PCIE#115

[66] CLKREQ_PCIE#116

[66] CLKREQ_PCIE#117

[66] CLKREQ_PCIE#118

[66] CLKREQ_PCIE#119

[66] CLKREQ_PCIE#120

[66] CLKREQ_PCIE#121

[66] CLKREQ_PCIE#122

[66] CLKREQ_PCIE#123

[66] CLKREQ_PCIE#124

[66] CLKREQ_PCIE#125

[66] CLKREQ_PCIE#126

[66] CLKREQ_PCIE#127

[66] CLKREQ_PCIE#128

[66] CLKREQ_PCIE#129

[66] CLKREQ_PCIE#130

[66] CLKREQ_PCIE#131

[66] CLKREQ_PCIE#132

[66] CLKREQ_PCIE#133

[66] CLKREQ_PCIE#134

[66] CLKREQ_PCIE#135

[66] CLKREQ_PCIE#136

[66] CLKREQ_PCIE#137

[66] CLKREQ_PCIE#138

[66] CLKREQ_PCIE#139

[66] CLKREQ_PCIE#140

[66] CLKREQ_PCIE#141

[66] CLKREQ_PCIE#142

[66] CLKREQ_PCIE#143

[66] CLKREQ_PCIE#144

[66] CLKREQ_PCIE#145

[66] CLKREQ_PCIE#146

[66] CLKREQ_PCIE#147

[66] CLKREQ_PCIE#148

[66] CLKREQ_PCIE#149

[66] CLKREQ_PCIE#150

[66] CLKREQ_PCIE#151

[66] CLKREQ_PCIE#152

[66] CLKREQ_PCIE#153

[66] CLKREQ_PCIE#154

[66] CLKREQ_PCIE#155

[66] CLKREQ_PCIE#156

[66] CLKREQ_PCIE#157

[66] CLKREQ_PCIE#158

[66] CLKREQ_PCIE#159

[66] CLKREQ_PCIE#160

[66] CLKREQ_PCIE#161

[66] CLKREQ_PCIE#162

[66] CLKREQ_PCIE#163

[66] CLKREQ_PCIE#164

[66] CLKREQ_PCIE#165

[66] CLKREQ_PCIE#166

[66] CLKREQ_PCIE#167

[66] CLKREQ_PCIE#168

[66] CLKREQ_PCIE#169

[66] CLKREQ_PCIE#170

[66] CLKREQ_PCIE#171

[66] CLKREQ_PCIE#172

[66] CLKREQ_PCIE#173

[66] CLKREQ_PCIE#174

[66] CLKREQ_PCIE#175

[66] CLKREQ_PCIE#176

[66] CLKREQ_PCIE#177

[66] CLKREQ_PCIE#178

[66] CLKREQ_PCIE#179

[66] CLKREQ_PCIE#180

[66] CLKREQ_PCIE#181

[66] CLKREQ_PCIE#182

[66] CLKREQ_PCIE#183

[66] CLKREQ_PCIE#184

[66] CLKREQ_PCIE#185

[66] CLKREQ_PCIE#186

[66] CLKREQ_PCIE#187

[66] CLKREQ_PCIE#188

[66] CLKREQ_PCIE#189

[66] CLKREQ_PCIE#190

[66] CLKREQ_PCIE#191

[66] CLKREQ_PCIE#192

[66] CLKREQ_PCIE#193

[66] CLKREQ_PCIE#194

[66] CLKREQ_PCIE#195

[66] CLKREQ_PCIE#196

[66] CLKREQ_PCIE#197

[66] CLKREQ_PCIE#198

[66] CLKREQ_PCIE#199

[66] CLKREQ_PCIE#200

[66] CLKREQ_PCIE#201

[66] CLKREQ_PCIE#202

[66] CLKREQ_PCIE#203

[66] CLKREQ_PCIE#204

[66] CLKREQ_PCIE#205

[66] CLKREQ_PCIE#206

[66] CLKREQ_PCIE#207

[66] CLKREQ_PCIE#208

[66] CLKREQ_PCIE#209

[66] CLKREQ_PCIE#210

[66] CLKREQ_PCIE#211

[66] CLKREQ_PCIE#212

[66] CLKREQ_PCIE#213

[66] CLKREQ_PCIE#214

[66] CLKREQ_PCIE#215

[66] CLKREQ_PCIE#216

[66] CLKREQ_PCIE#217

[66] CLKREQ_PCIE#218

[66] CLKREQ_PCIE#219

[66] CLKREQ_PCIE#220

[66] CLKREQ_PCIE#221

[66] CLKREQ_PCIE#222

[66] CLKREQ_PCIE#223

[66] CLKREQ_PCIE#224

[66] CLKREQ_PCIE#225

[66] CLKREQ_PCIE#226

[66] CLKREQ_PCIE#227

[66] CLKREQ_PCIE#228

[66] CLKREQ_PCIE#229

[66] CLKREQ_PCIE#230

[66] CLKREQ_PCIE#231

[66] CLKREQ_PCIE#232

[66] CLKREQ_PCIE#233

[66] CLKREQ_PCIE#234

[66] CLKREQ_PCIE#235

[66] CLKREQ_PCIE#236

[66] CLKREQ_PCIE#237

[66] CLKREQ_PCIE#238

[66] CLKREQ_PCIE#239

[66] CLKREQ_PCIE#240

[66] CLKREQ_PCIE#241

[66] CLKREQ_PCIE#242

[66] CLKREQ_PCIE#243

[66] CLKREQ_PCIE#244

[66] CLKREQ_PCIE#245

[66] CLKREQ_PCIE#246

[66] CLKREQ_PCIE#247

[66] CLKREQ_PCIE#248

[66] CLKREQ_PCIE#249

[66] CLKREQ_PCIE#250

[66] CLKREQ_PCIE#251

[66] CLKREQ_PCIE#252

[66] CLKREQ_PCIE#253

[66] CLKREQ_PCIE#254

[66] CLKREQ_PCIE#255

[66] CLKREQ_PCIE#256

[66] CLKREQ_PCIE#257

[66] CLKREQ_PCIE#258

[66] CLKREQ_PCIE#259

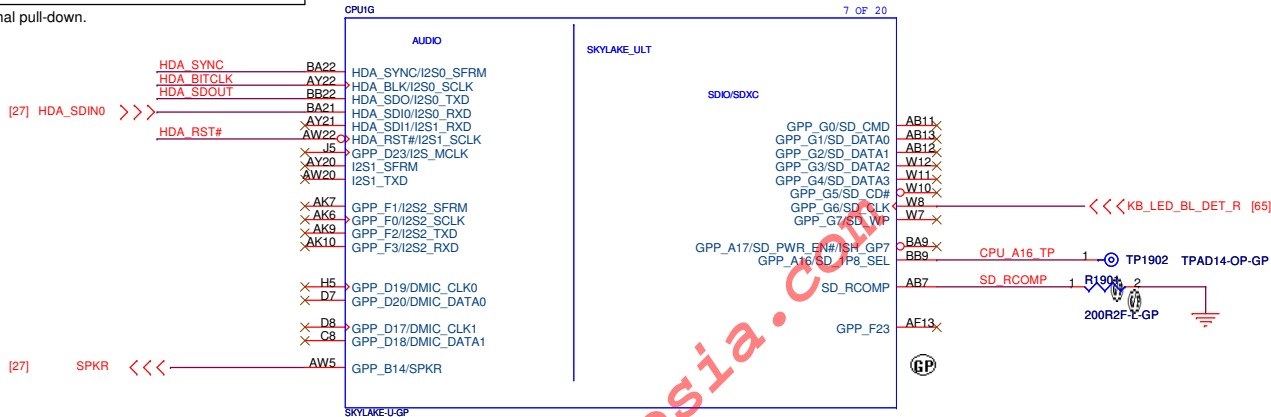
[66] CLKREQ_PCIE#260

Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.



PCH strap pin:

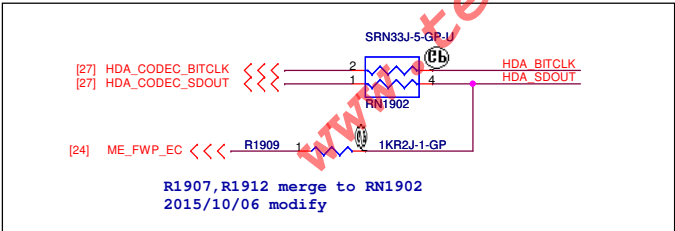
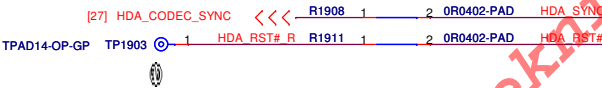
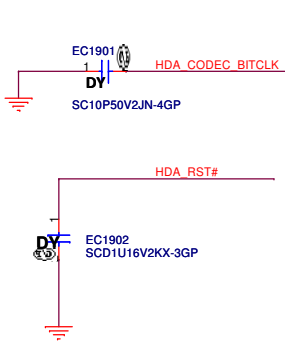
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

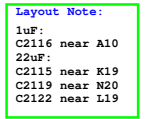
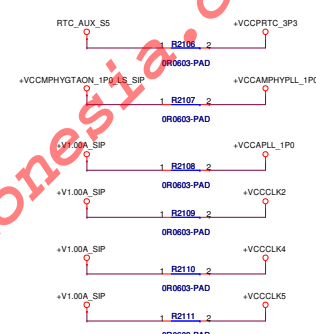
PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

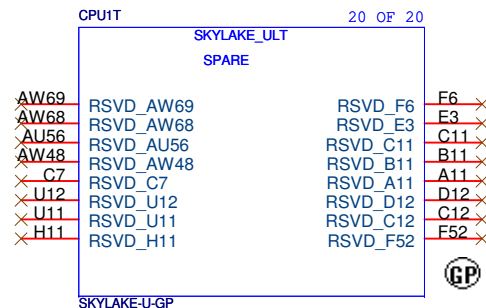
The internal pull-down is disabled after PLTRST# deasserts



<Core Design>




Main Func = PCH



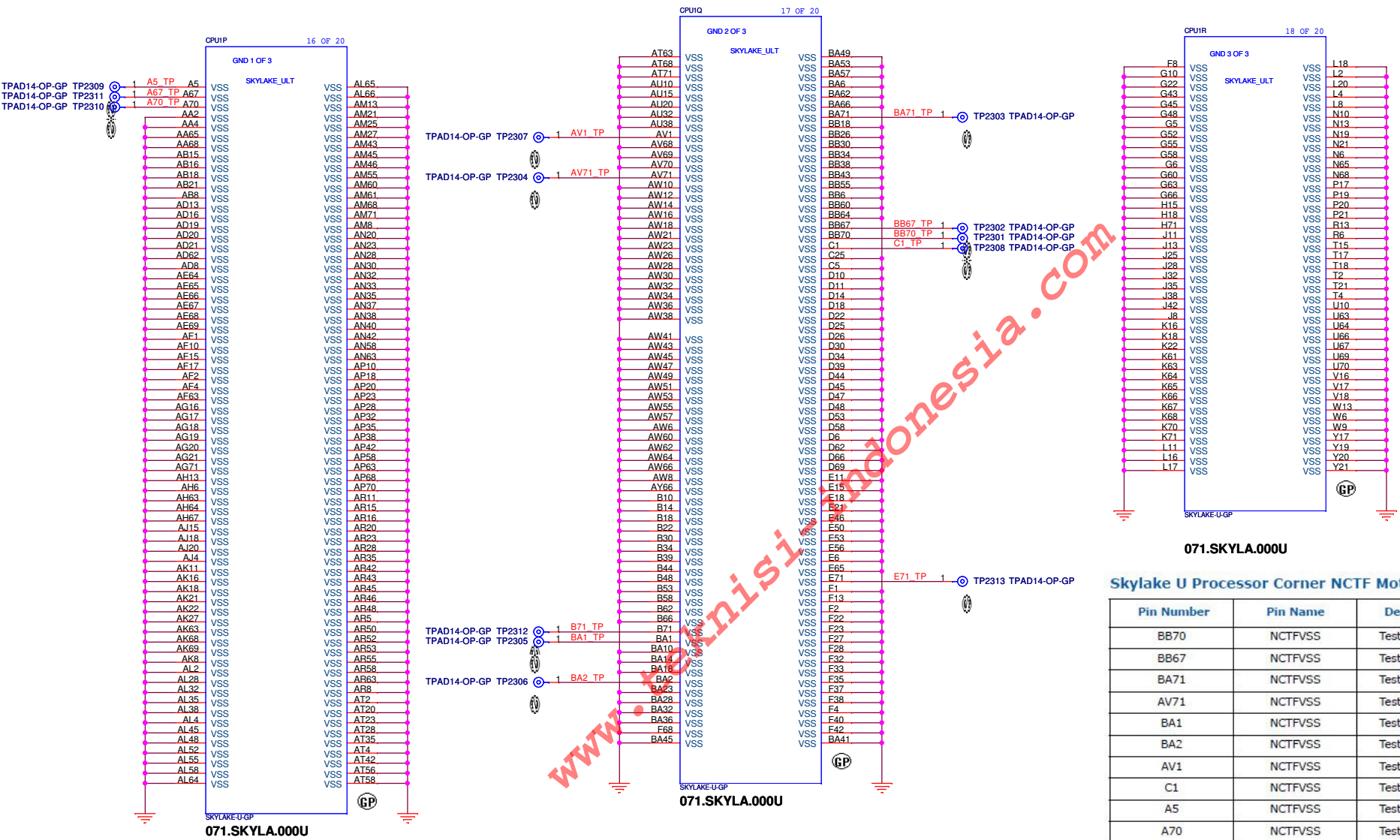
071.SKYLA.000U

www.teknisi-indonesia.com

<Core Design>

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU (RSVD)					
Size A4	Document Number Starload SKL-U				Rev A00
Date: Thursday, February 18, 2016			Sheet 22 of 106		


Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

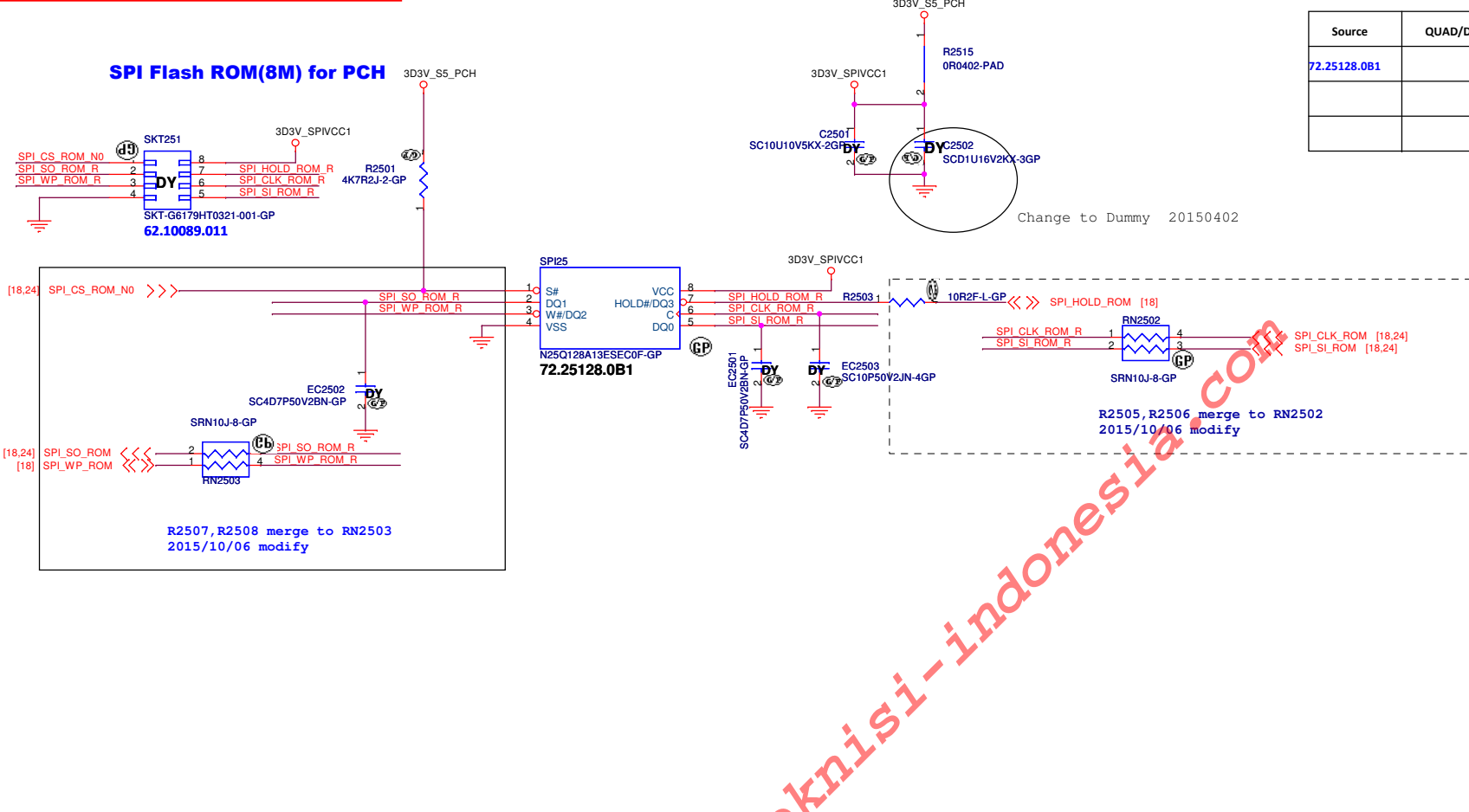
CPU (VSS)

Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016

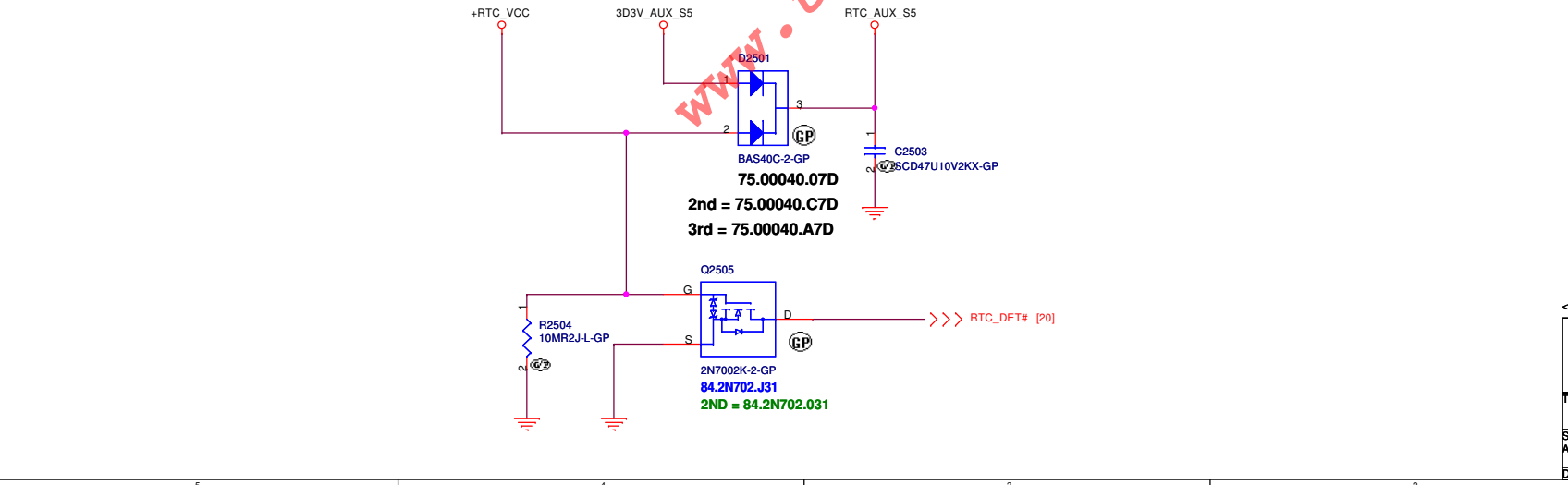
Sheet 23 of 106

Main Func = SPI Flash




Source	QUAD/DUAL fast read	DUAL fast read	SFDP
72.25128.0B1	O	O	O
	O	O	O
	O	O	O

Main Func = RTC



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

TitleFlash/RTC

SizeA3

Document NumberStarload SKL-U

RevA00

Date: Thursday, February 25, 2016Sheet 25 of 106

www.teknisi-indonesia.com

Main Func = Audio

(Blanking)

www.teknisi-indonesia.com

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Starload SKL-U		Rev A00
Date: Thursday, February 18, 2016		Sheet 30 of	106

(Blanking)

www.teknisi-indonesia.com

Main Func = LAN

(Blanking)

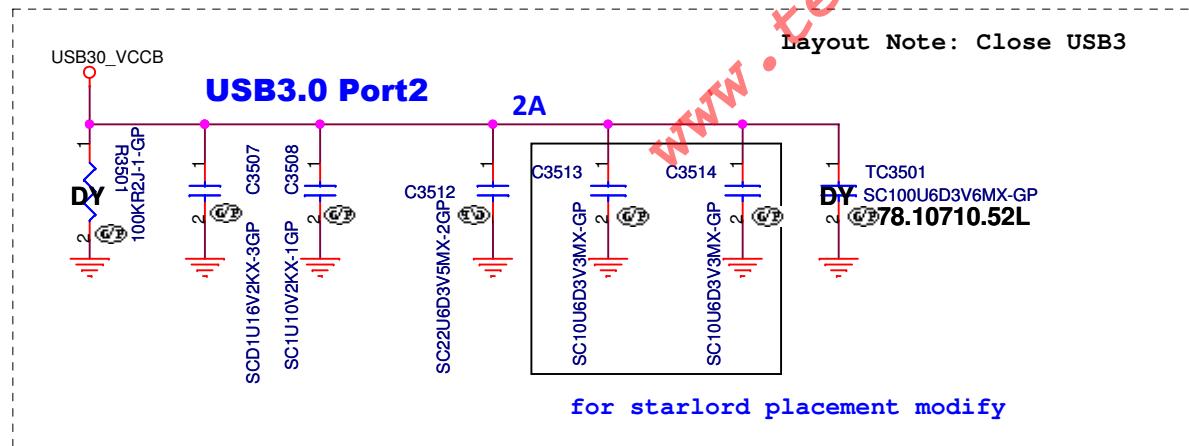
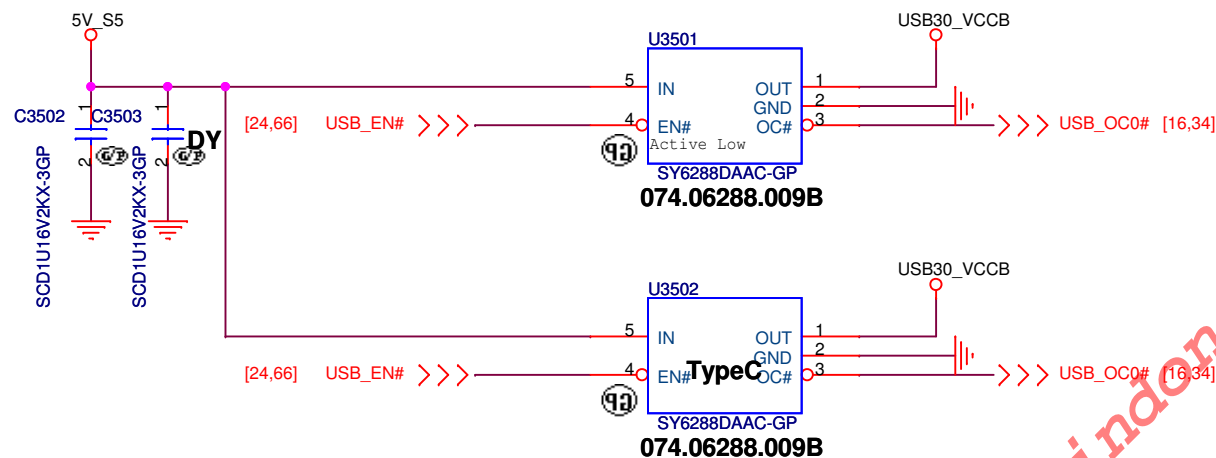
www.teknisi-indonesia.com

5
Main Func = Card Reader

(Blanking)

www.teknisi-indonesia.com

Main Func = USB3.0 Port1



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB switch

Size

Document Number

Starload SKL-U

Rev

A00

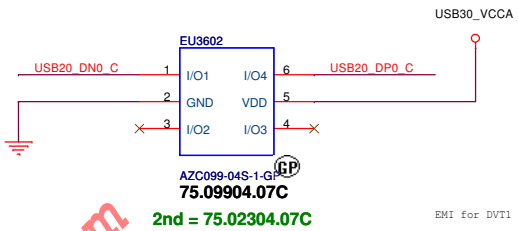
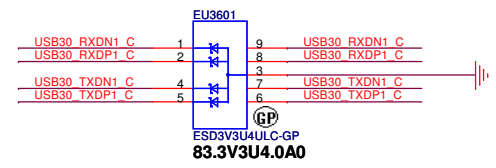
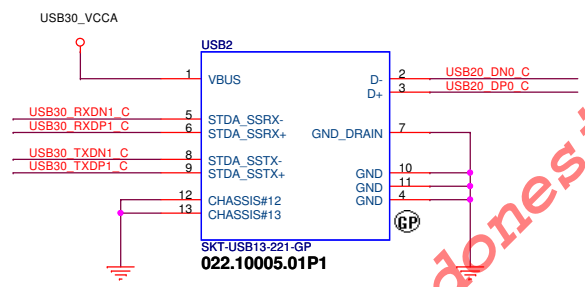
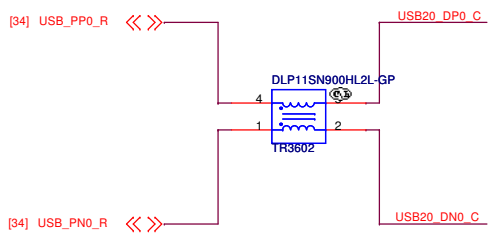
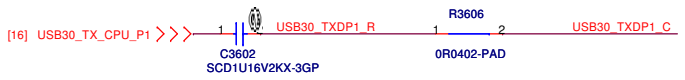
Date: Thursday, February 25, 2016

Sheet 35 of 106

Main Func = USB3.0 Port1

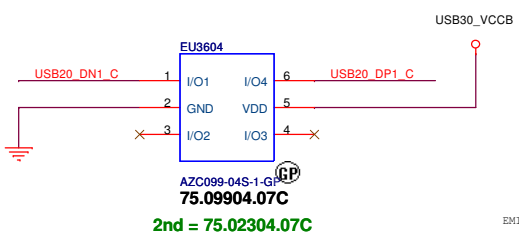
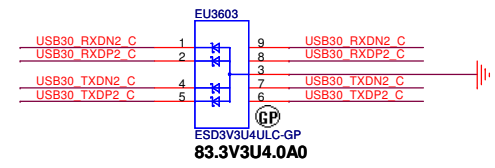
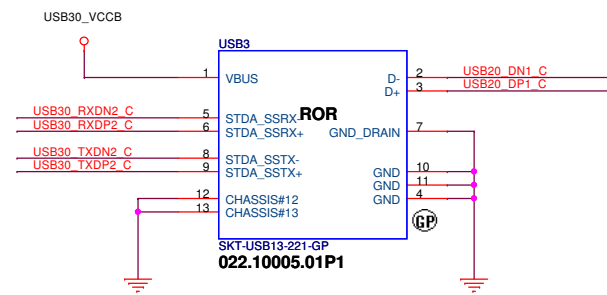
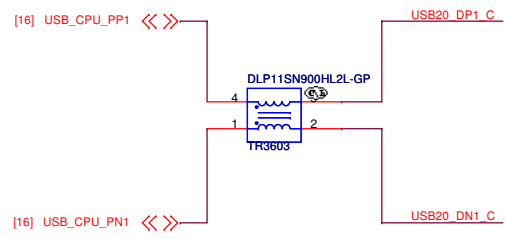
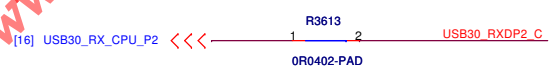
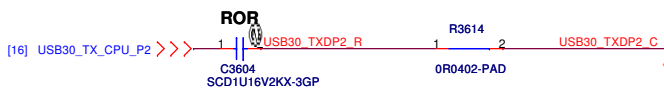
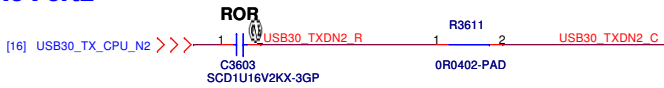
USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port2



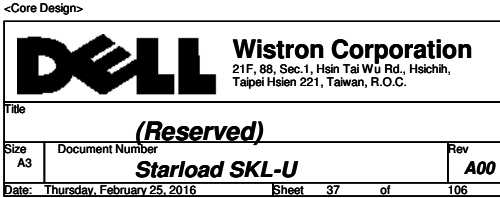
<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

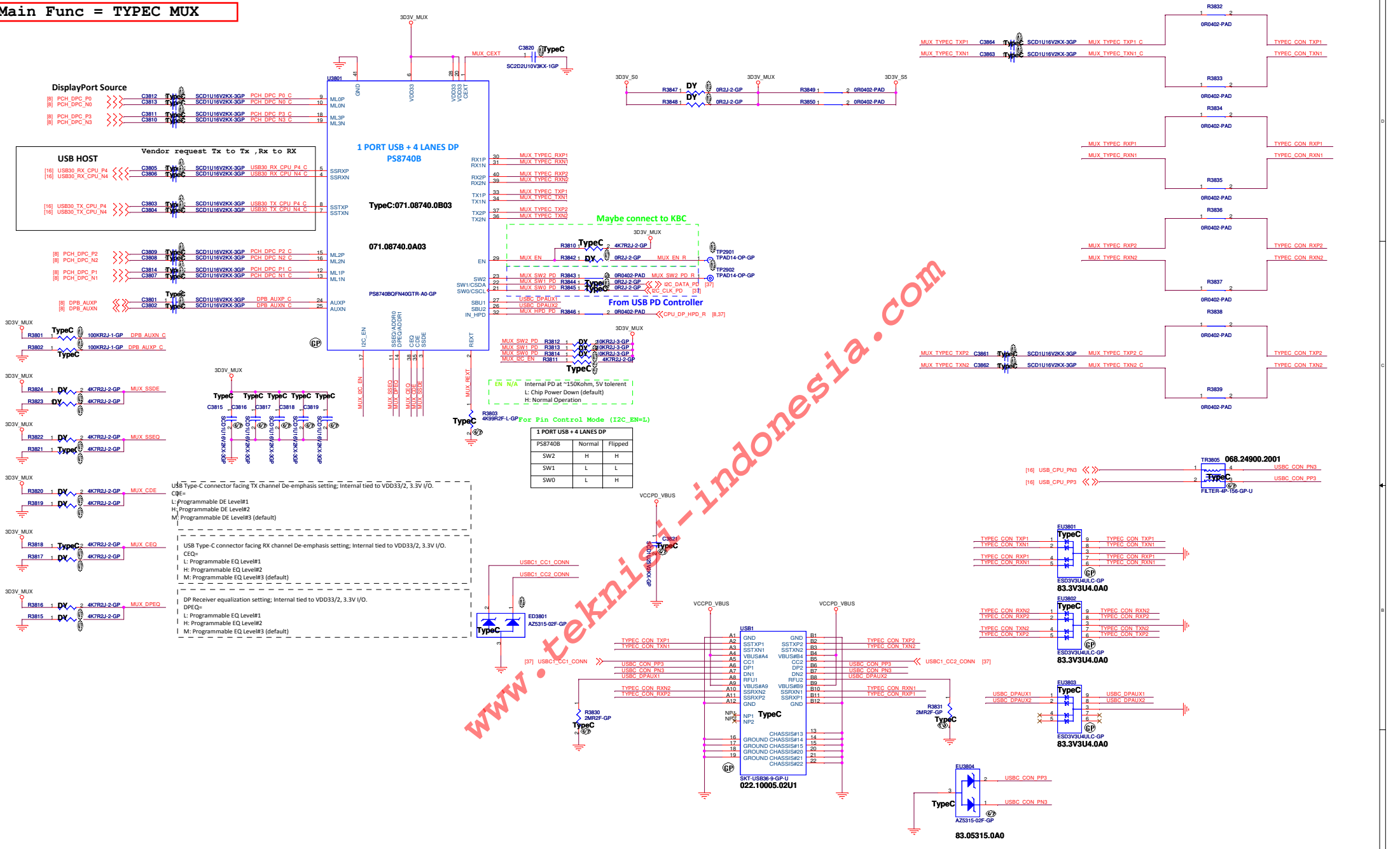
Title: **USB30**

Size: A3 Document Number: **Starload SKL-U** Rev: **A00**

Date: Thursday, February 25, 2016 Sheet 36 of 106

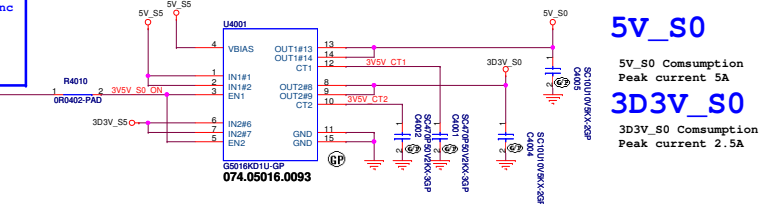


Main Func = TYPEC MUX



ROSA Run Power

Remove Q4001 & R4004 by Hsync 20150417

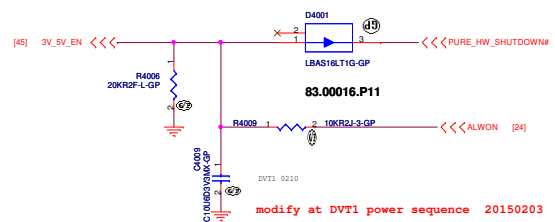


5V_S0

5V_S0 Consumption
Peak current 5A

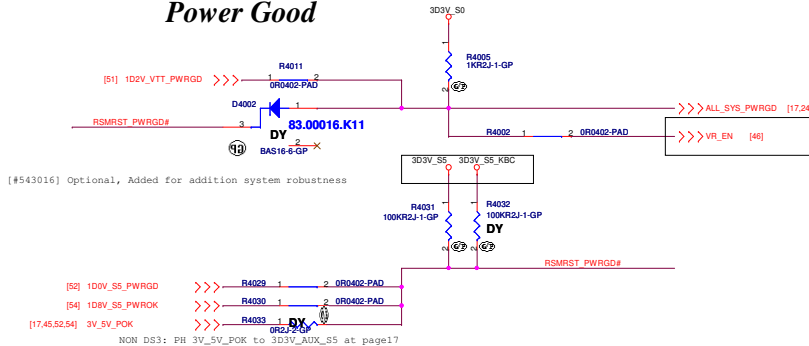
3D3V_S0

3D3V_S0 Consumption
Peak current 2.5A

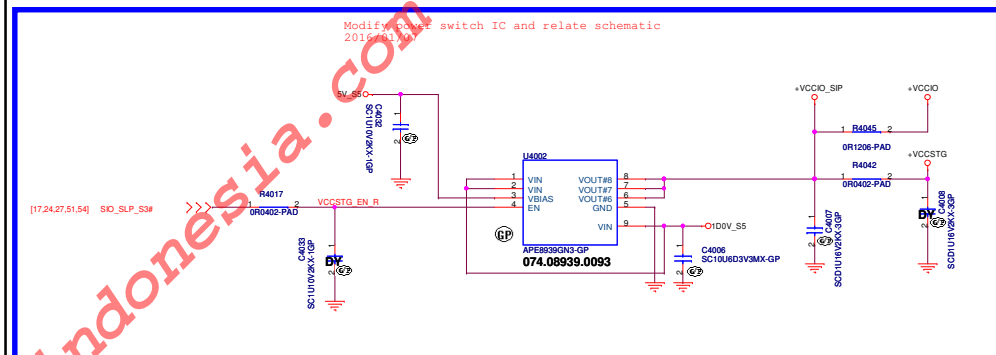


20150116 2032

Power Good

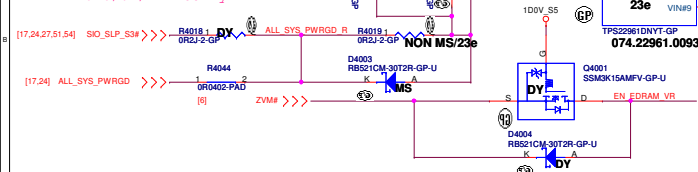


VCCIO and VCCSTG



EOPIO and EDRAM

[#543977 Rev1.1] PDDG change to ALL_SYS_PWRGD 2016/02/24 modify



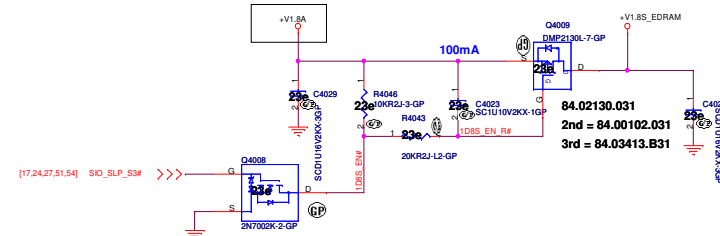
+V_EDRAM_VR

Voltage = 1.0 V ± 50 mV
Imax = 3.2 A
TRISE = 240 us

+V_EOPIO_VR

Voltage = 1.0 V ± 50 mV
Imax = 2.8 A
TRISE = 240 us

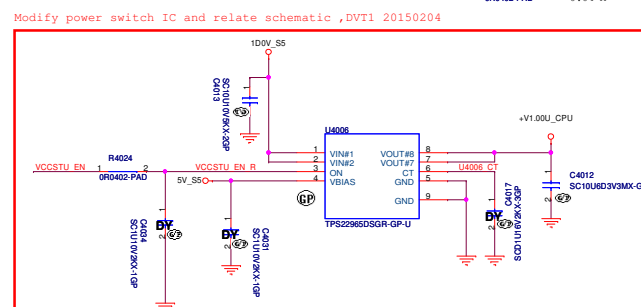
V1.8S



MANAGEMENT RAIL POWER GENERATION

VCCST, VCCIO, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

VCCST



Core Design

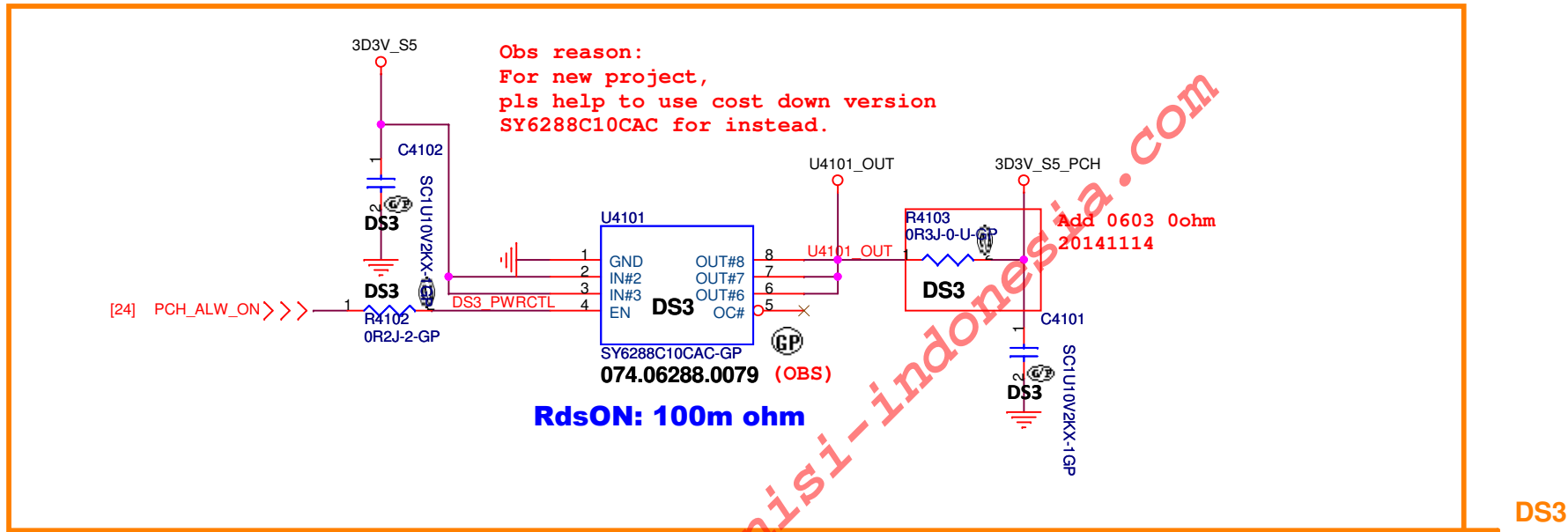
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsueh,
Taipei Hsien 221, Taiwan, R.O.C.

Power Plane Enable

Starload SKL-U

Rev A00

Main Func = Power Plane & Sequence



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Connected_Standby(1/2)+DS3

Size
A4

Document Number

Starload SKL-U

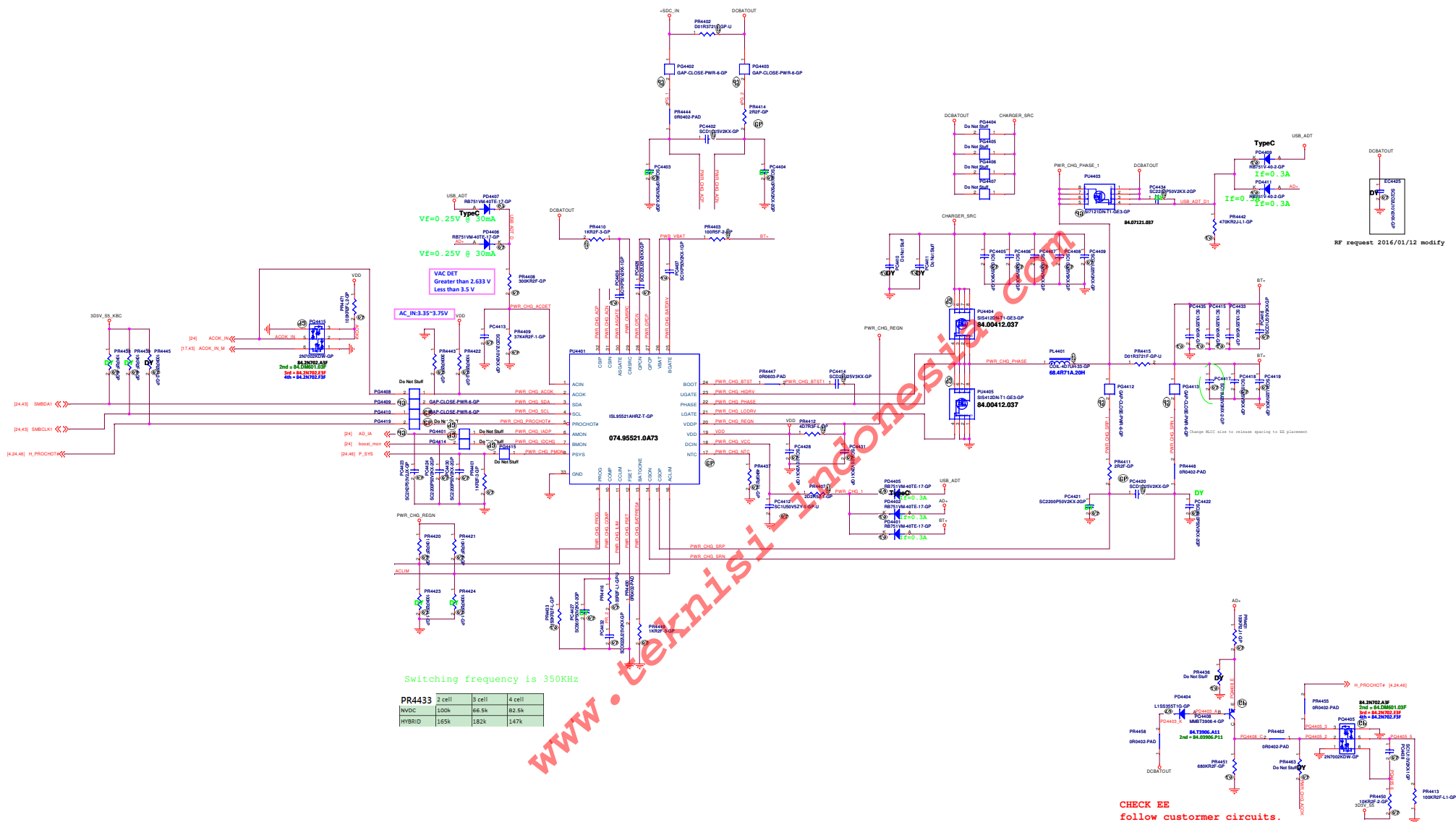
Rev
A00

Date: Thursday, February 25, 2016

Sheet 41 of 106

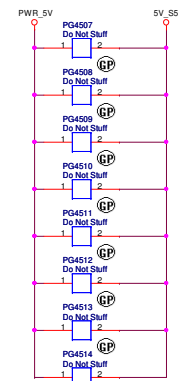
Main Func = DIMM1
Main Func = DIMM2

www.teknisi-indonesia.com

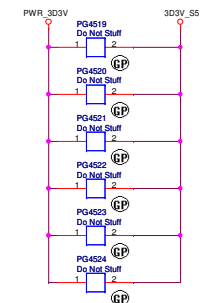


CHECK EE
follow customer circuits.

```
SSID = PWR.Plane.Regulator_3D3V
```



Design Current=5A
7.5A<OCP>9A

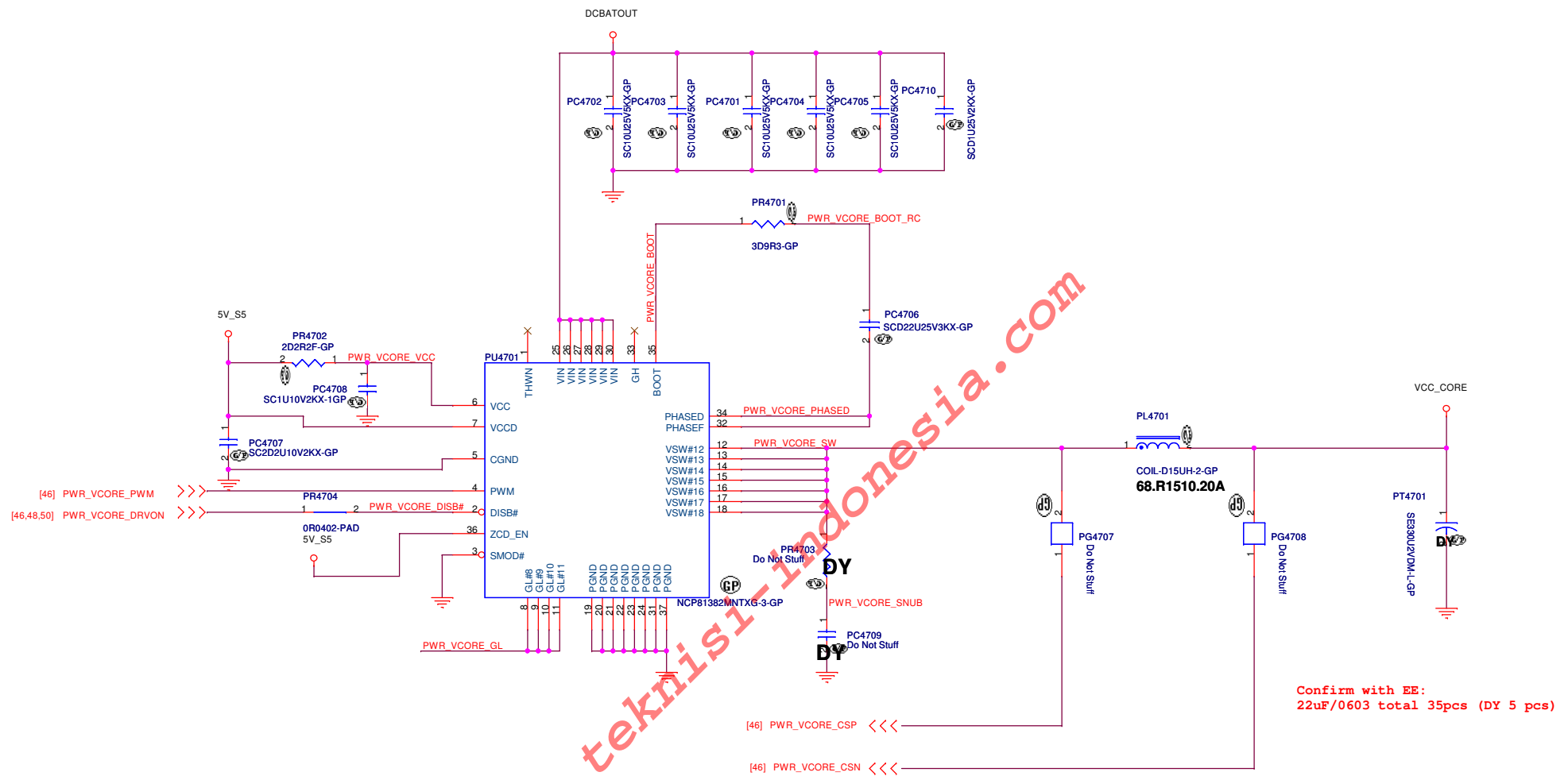


<Core Design>



RF request 2016/01/12 modify


```
Main Func = CPU_CORE
```



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Author	Year	Journal	Volume	Page
...

NCP81382MN_CPU_VCORE(2/3)Size
A3

Document Number

ment Number
Starload SKL-U

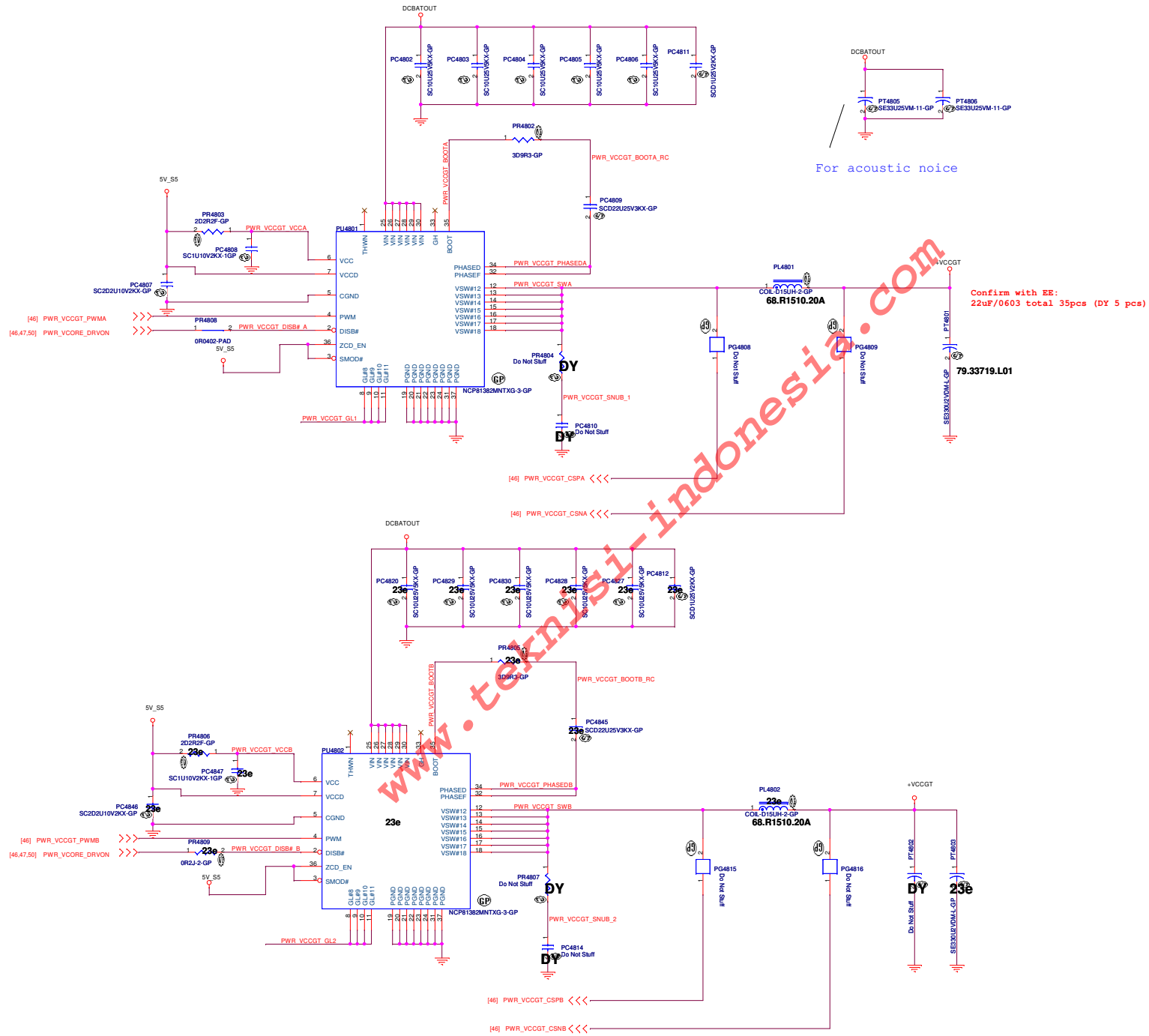
Rev

A00

Date: Thursday, February 25, 2016

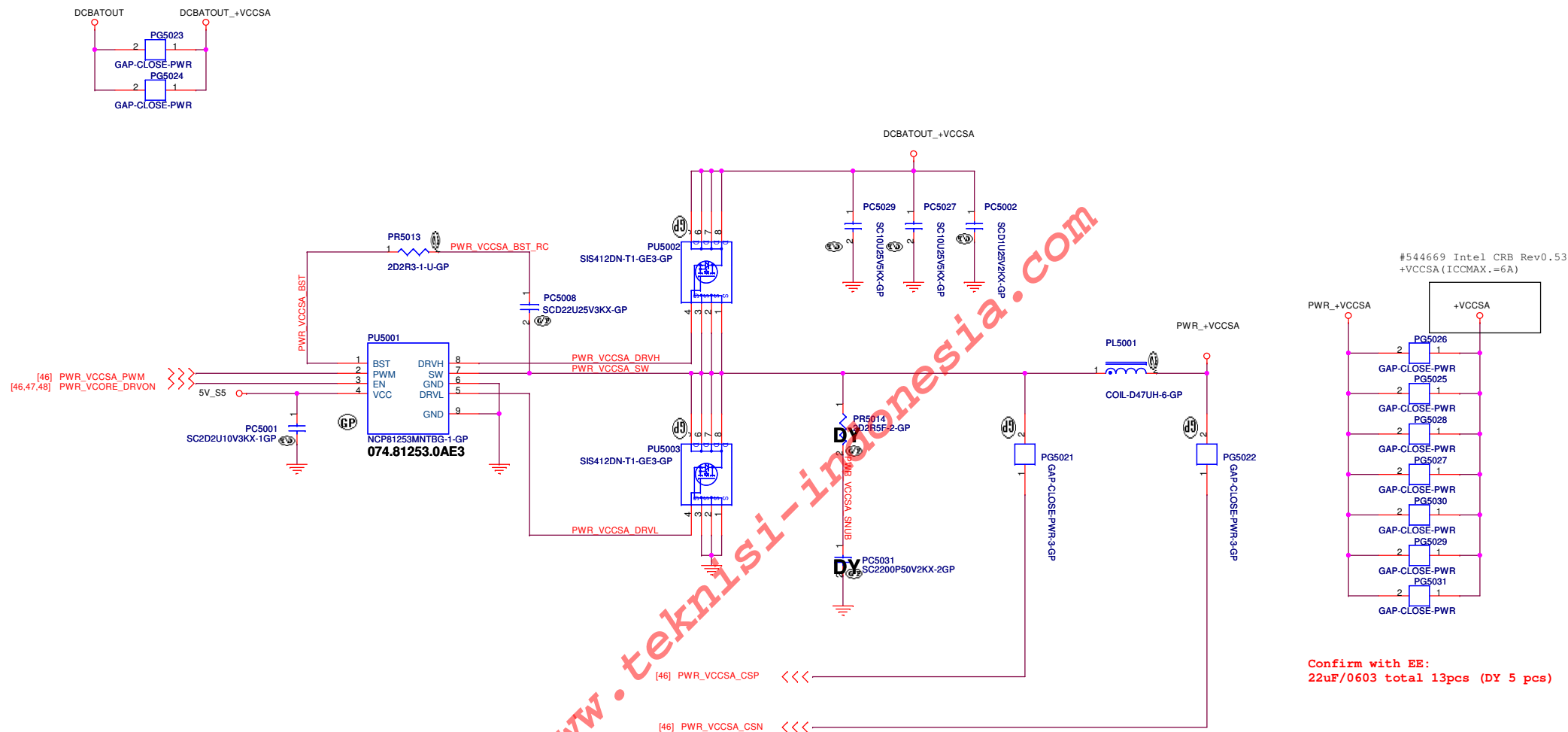
Sheet 47 of 106

Main Func = CPU_CORE



www.teknisi-indonesia.com

Main Func = CPU_CORE

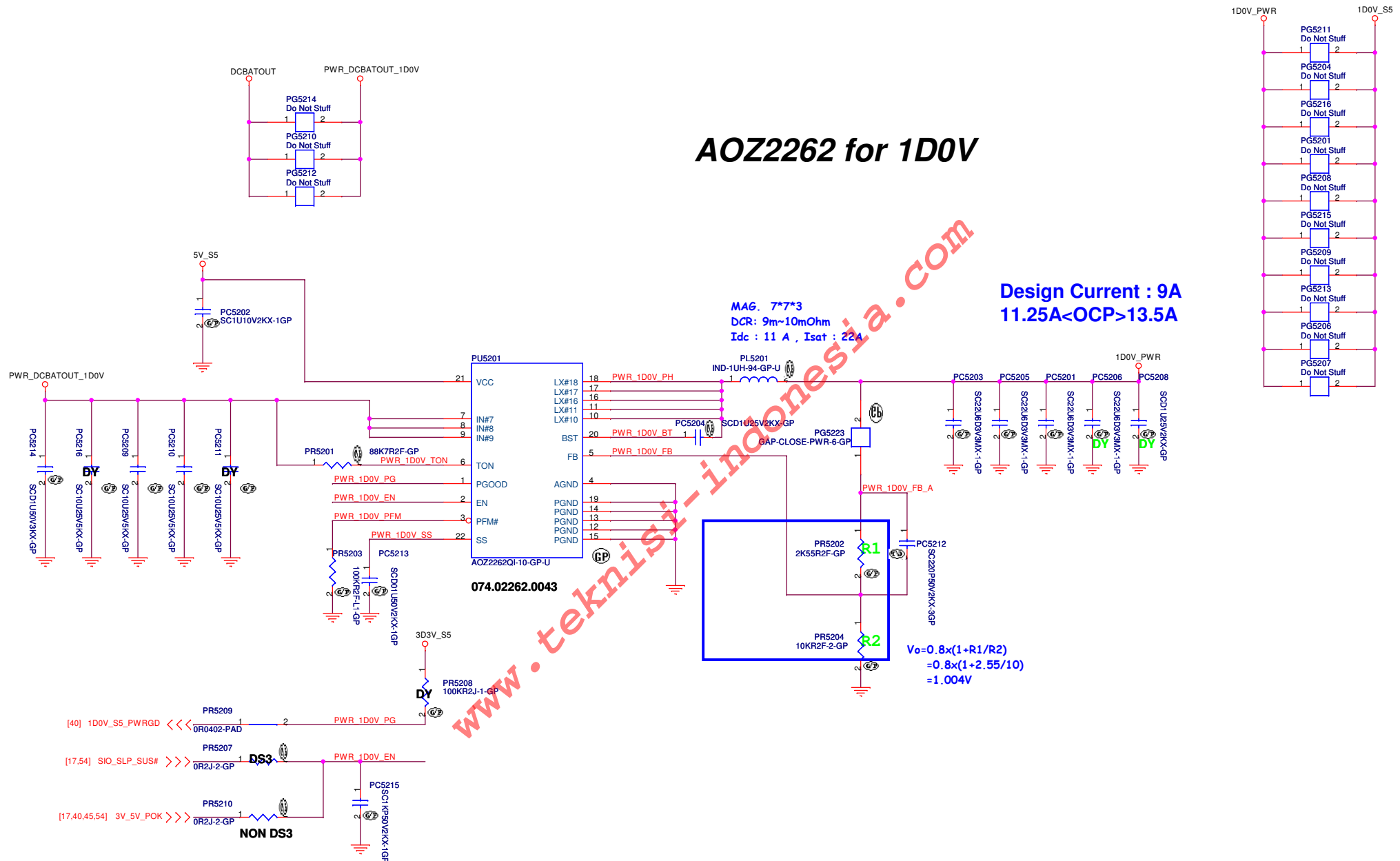


Confirm with EE:
22uF/0603 total 13pcs (DY 5 pcs)


```
SSID = PWR.Plane.Regulator_1D0V
```

AOZ2262 for 1D0V

Design Current : 9A
11.25A<OCP>13.5A



<Core Design>




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
(Reserved)			
Size A3	Document Number Starload SKL-U	Rev A00	
Date: Thursday, February 25, 2016		Sheet 52 of	106

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

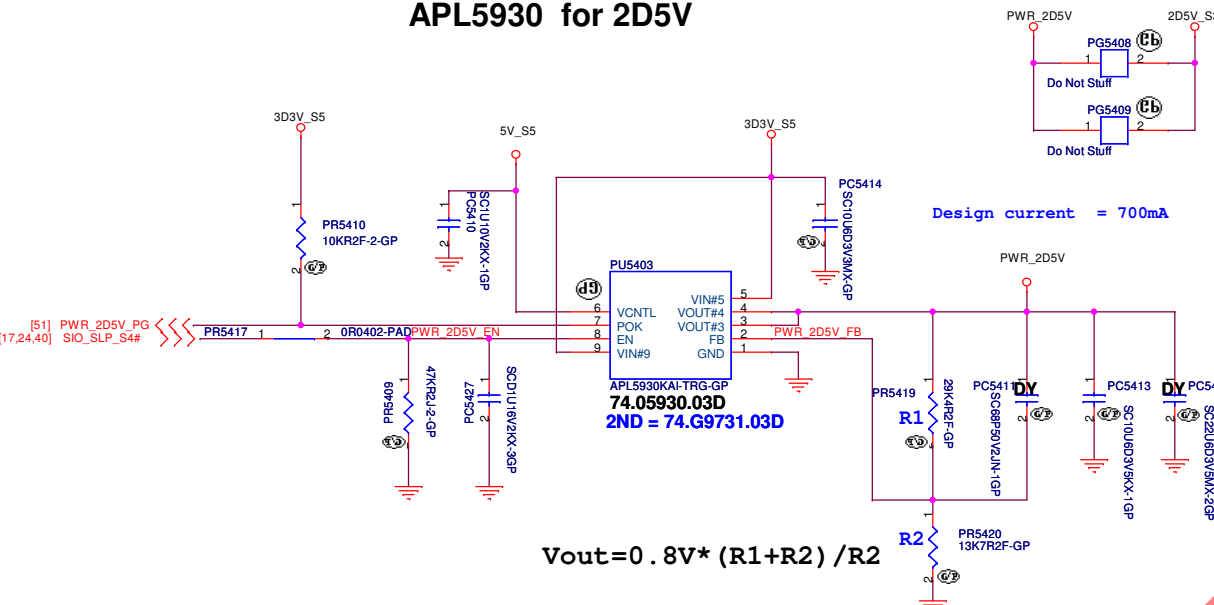
(Reserved)

Size	Document Number	Rev
A3	Starload SKL-U	A00

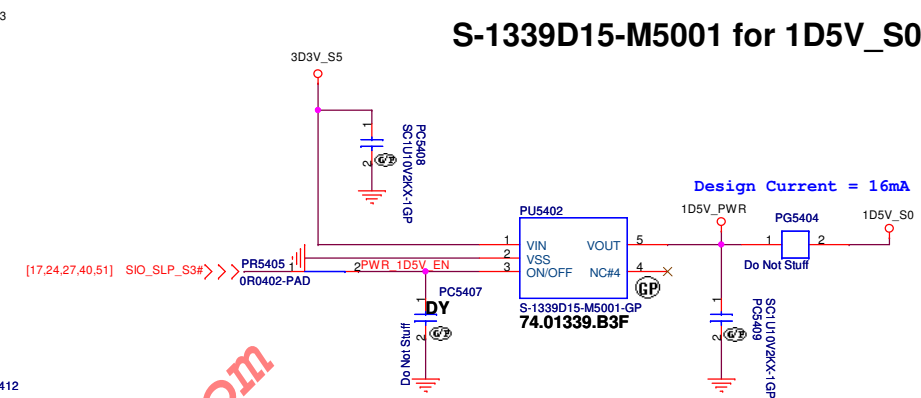
Date: Thursday, February 18, 2016	Sheet 53 of 106
-----------------------------------	-----------------

Main Func = 1D5V

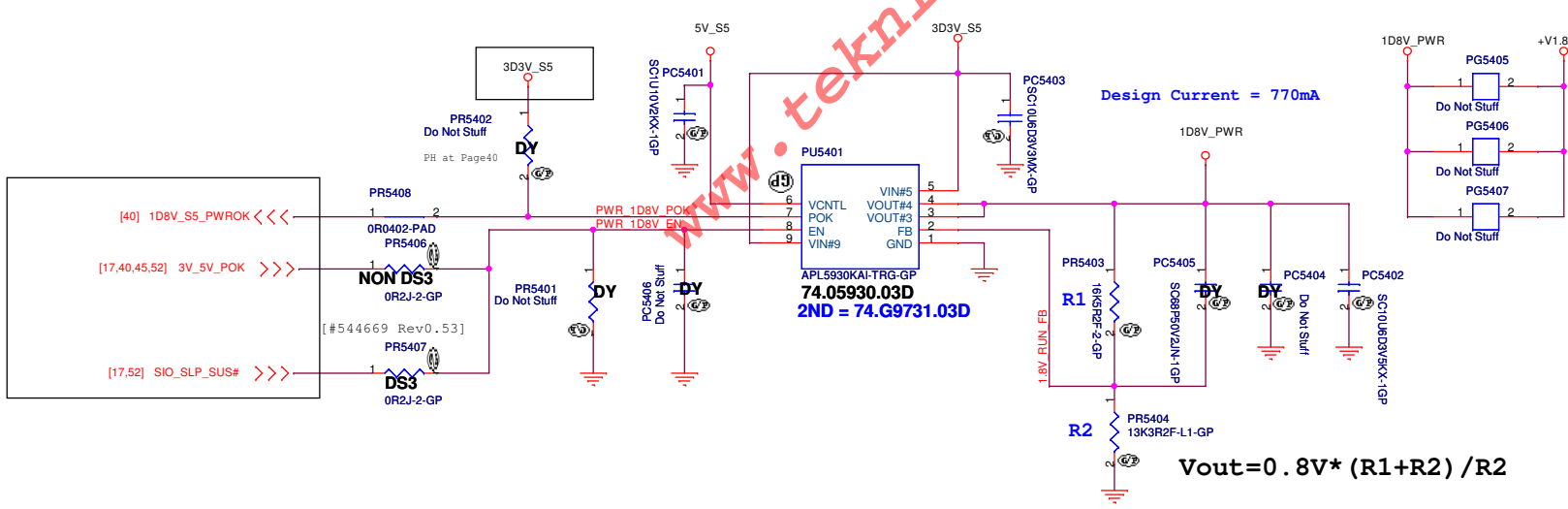
APL5930 for 2D5V



S-1339D15-M5001 for 1D5V_S0



APL5930 for 1D8V_S5



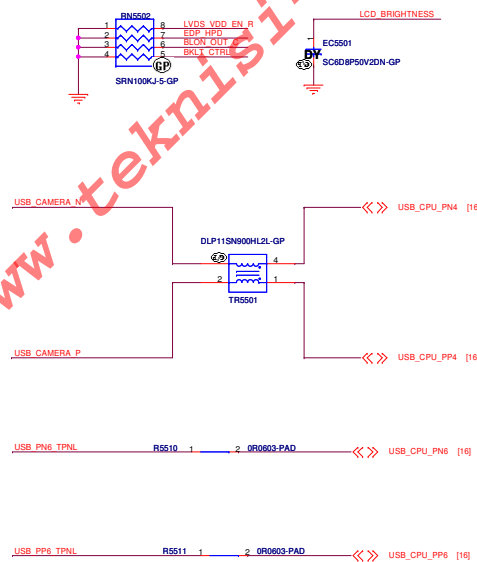
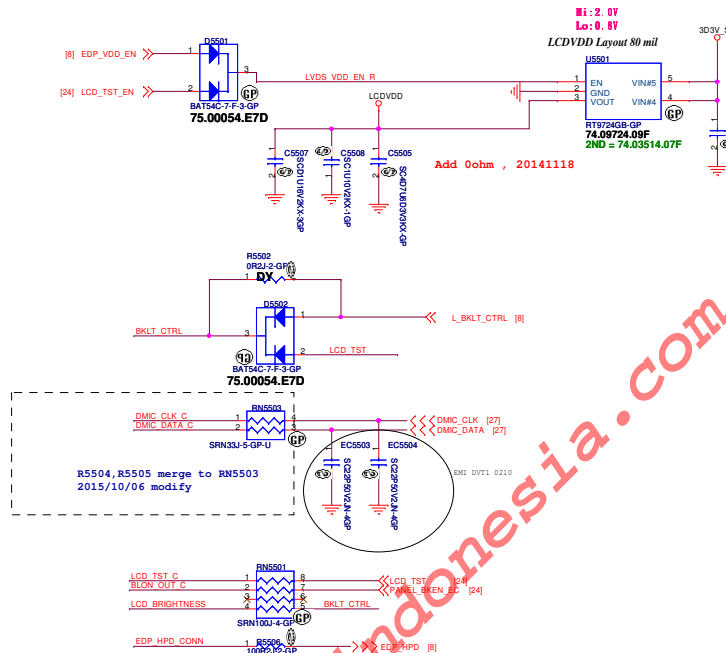
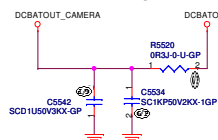
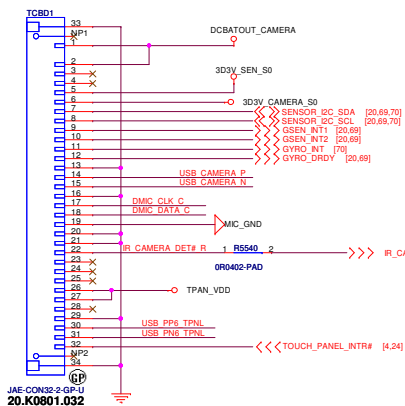
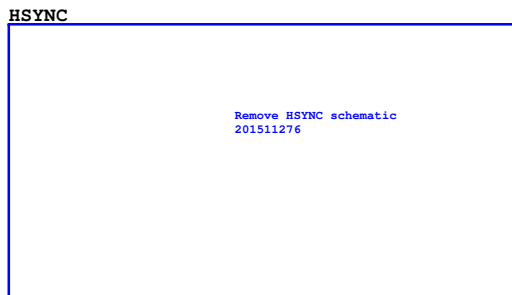
<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

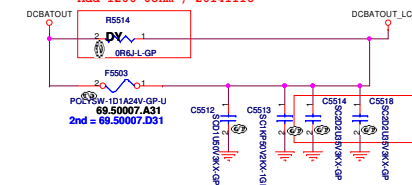
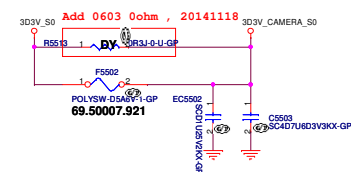
Title (Reserved)

Size A3	Document Number Starload SKL-U	Rev A00
---------	--------------------------------	---------

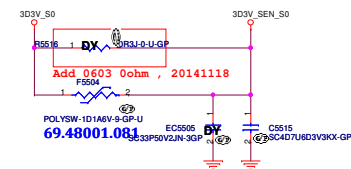
Date: Thursday, February 25, 2016 Sheet 54 of 106



SENSOR POWER




Starload height limite change to 0603 package
2015/09/24 modify

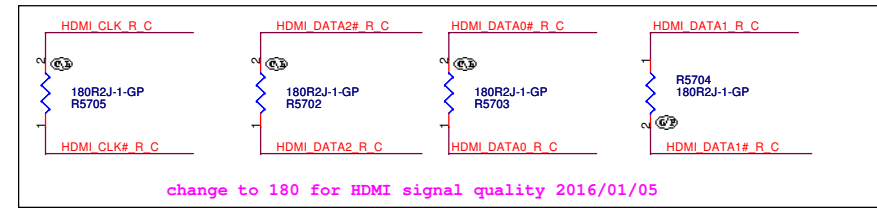
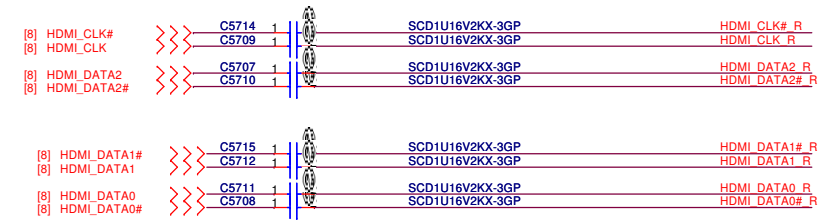
[illegible]

Starload height limite change to 0603 package
2015/09/30 modify

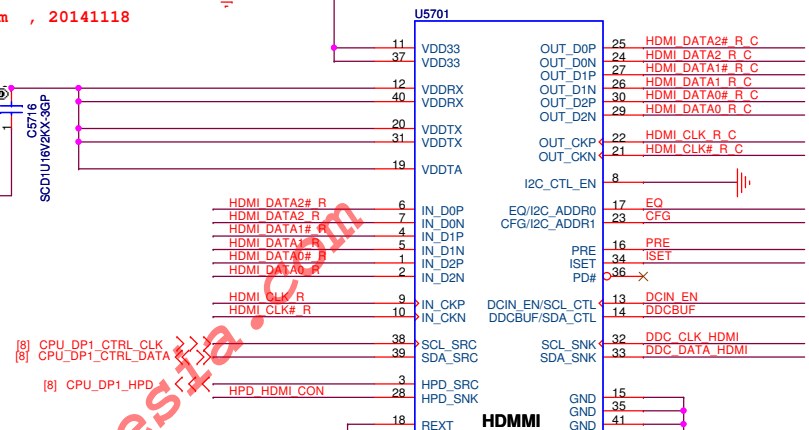
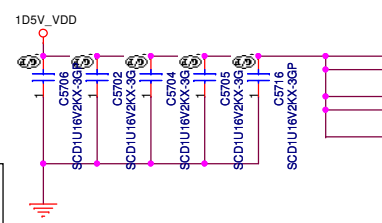
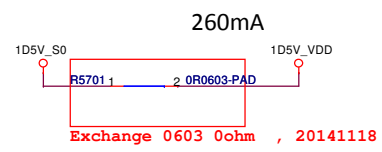
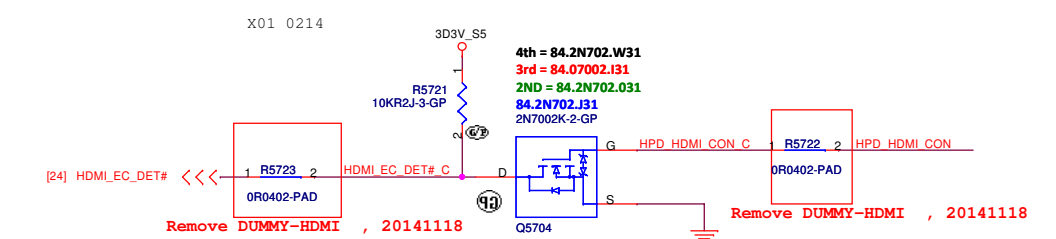
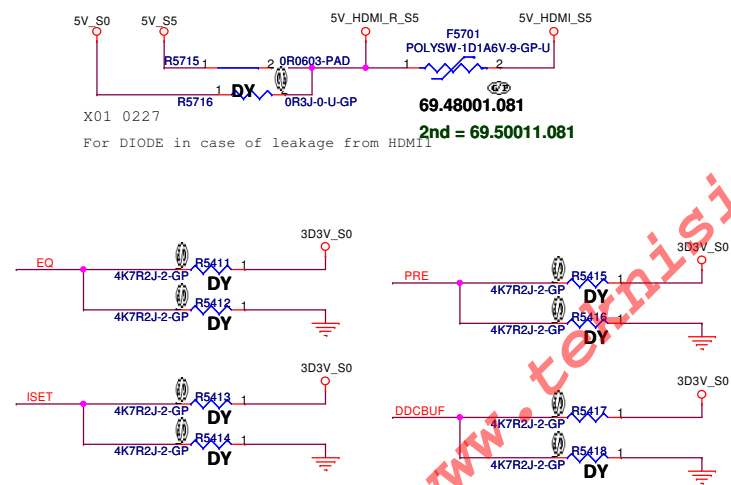
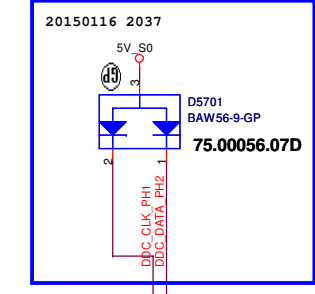
www.teknisi-indonesia.com

<Core Design>		
		
Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshien, Taipei Hsien 221, Taiwan, R.O.C.		
Title CRT		
Size A2	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2010 Sheet 66 of 106		

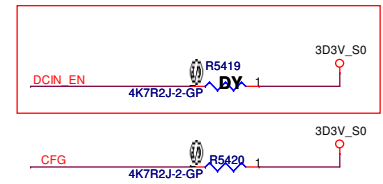
Main Func = HDMI



Change symbol part number, because origin symbol is DELL OBS part



Vendor suggest, Dummy for floating
20141117




Remove DUMMY-HDMI , 20141118

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A3

Document Number

Starload SKL-U

Rev

A00


Date: Thursday, February 18, 2016

Sheet 58 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A3

Document Number

Starload SKL-U

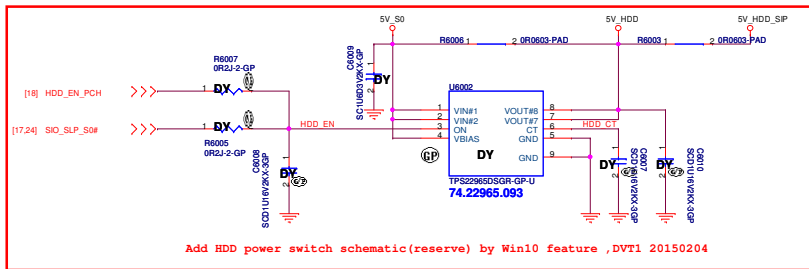
Rev

A00

Date: Thursday, February 18, 2016

Sheet 59 of 106

SATA HDD Connector



Modify at 20150922

SV_HDD_SIP

2 GR0803-PAD

www.teknisi-indonesia.com

Main Func = WLAN

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

NGFF WLAN CONN


Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016	Sheet 61 of 106
-----------------------------------	-----------------

(Blanking)

www.teknisi-indonesia.com

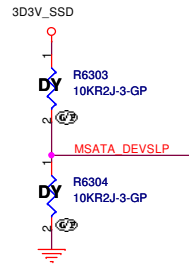
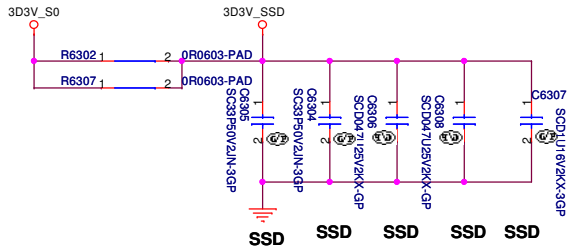
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number Starload SKL-U		Rev A00
Date: Thursday, February 18, 2016		Sheet 62 of	106

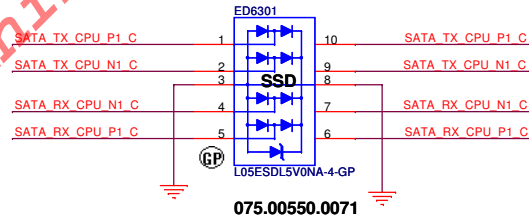
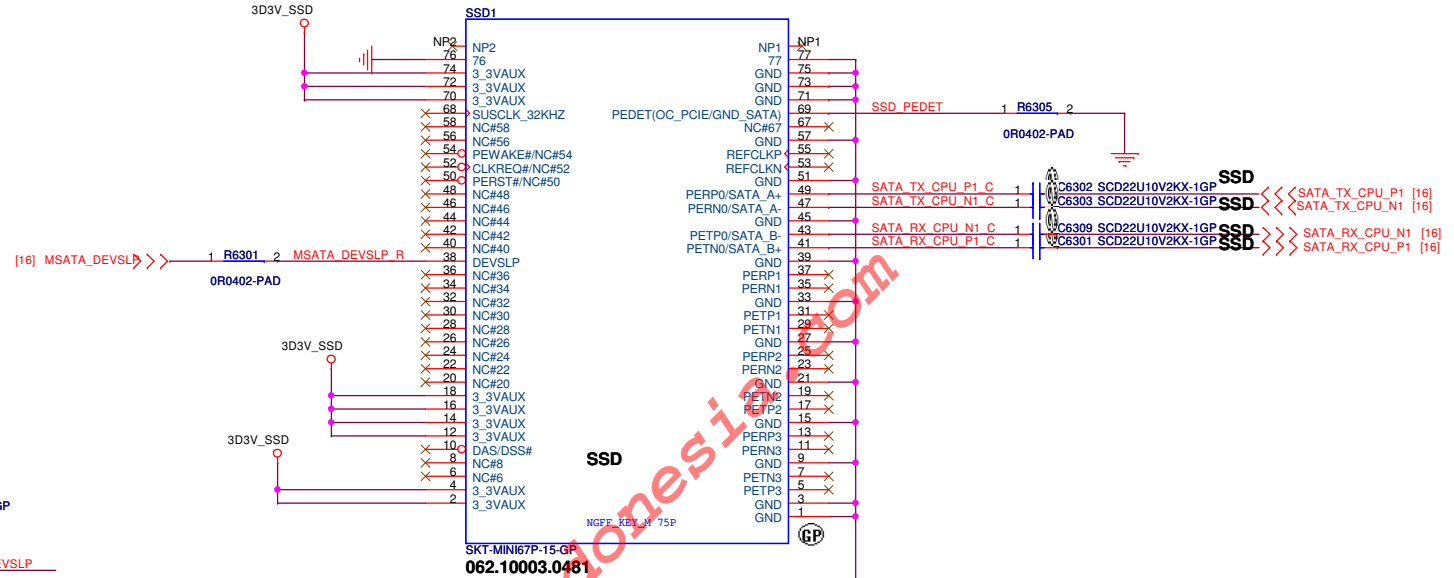
SSD M.2

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to signal an exit from DEVSLP state.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.



SSD M.2 CONN



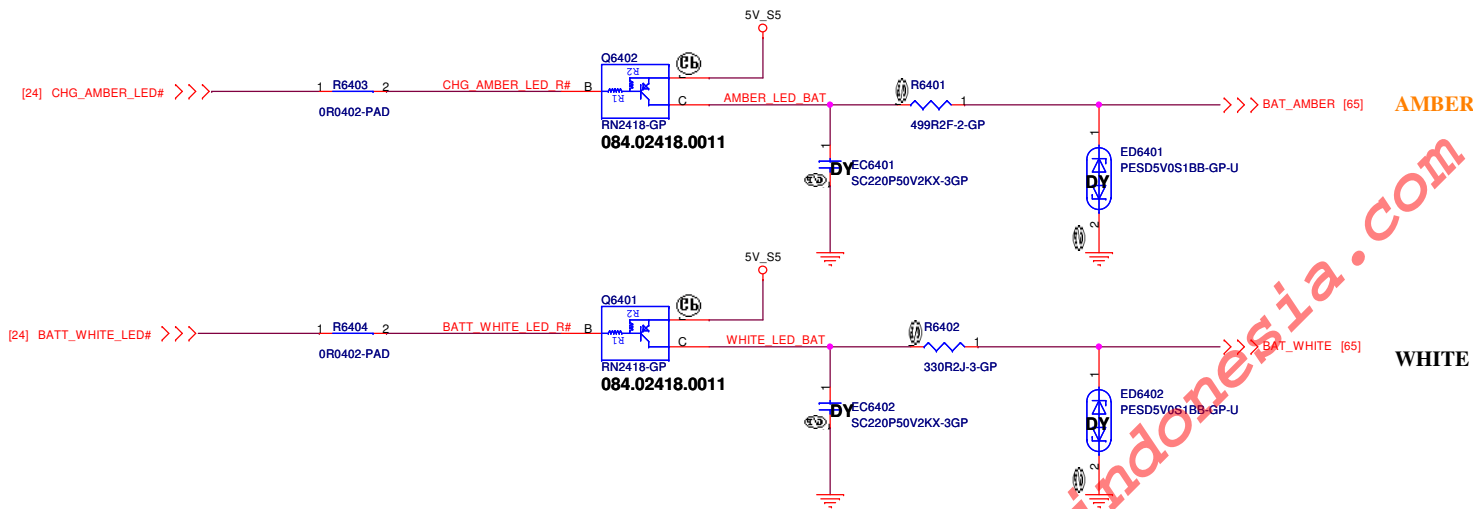
<Core Design>



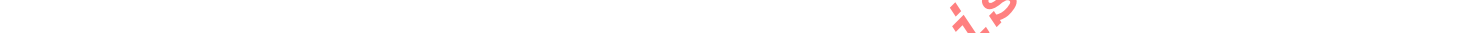
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title (Reserved)		
Size A3	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 25, 2016		
Sheet 63 of 106		

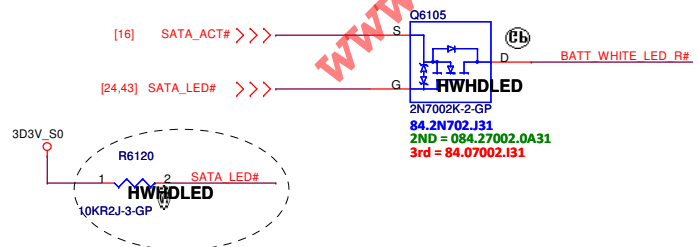
Battery LED1 (AMBER_LED)
Low activated from KBC GPIO



Battery LED2 (WHITE_LED)
Low activated from KBC GPIO

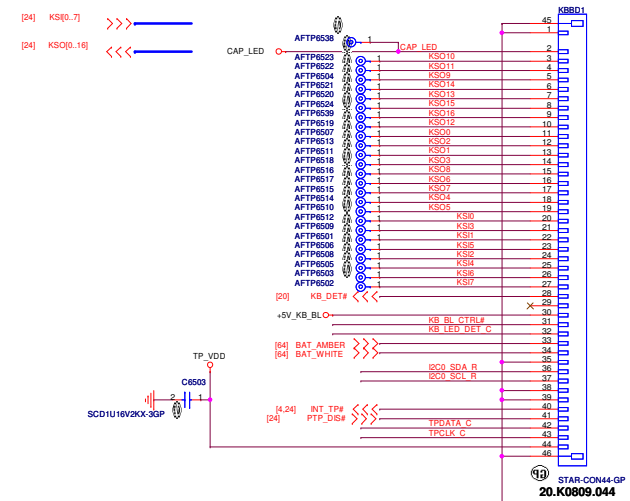


SATA LED



Add SATA LED solution by customer request 2016/02/03

Keyboard



5V_S0

69.50007.921

POLYSW-DS66-0-UP

KBBL

R6501

DY

OR3J-0-U-GP

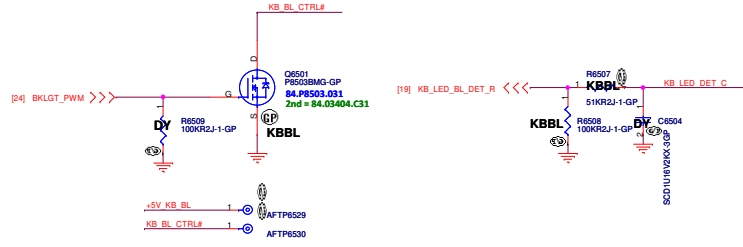
5V_KB_BL

C6501

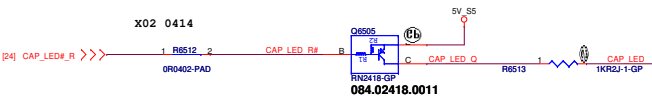
KBBL

SCD1U16V2KX-3GP

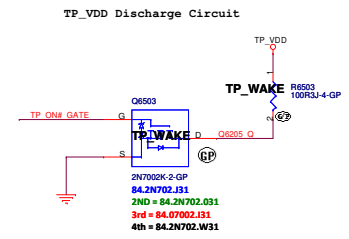
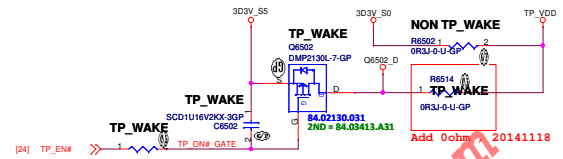
KB Backlight Power Consumption: 285mA max.



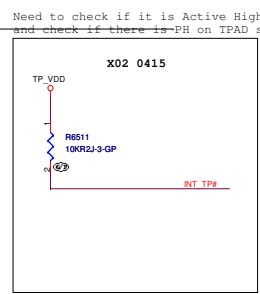
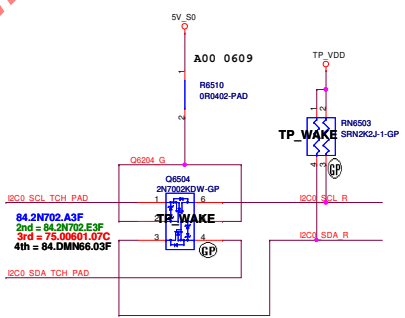
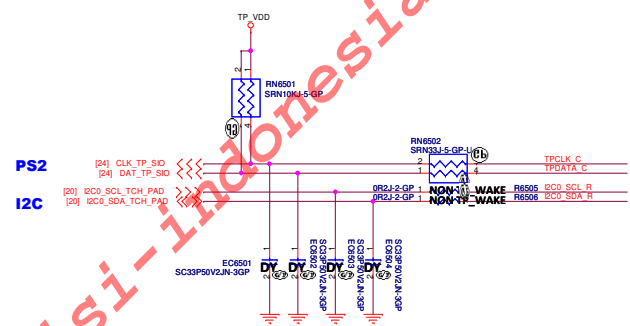
CAP LED Control
LOW actived from KBC GPIO



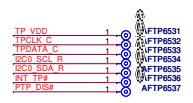
3
Main Func = TPAD



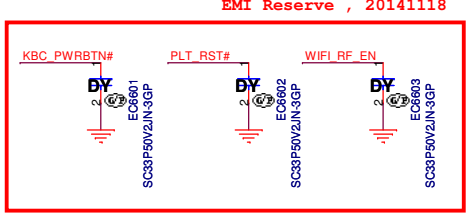
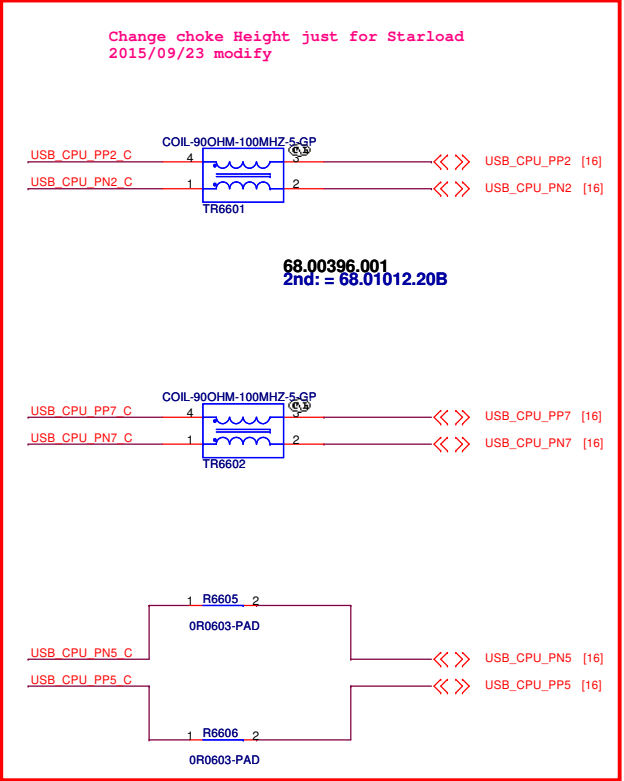
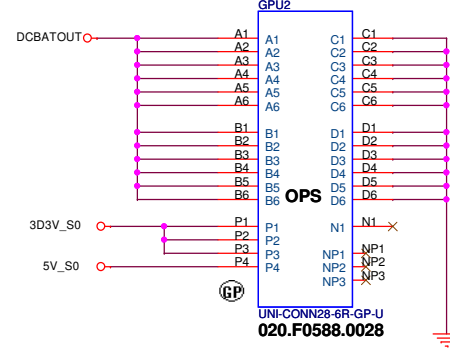
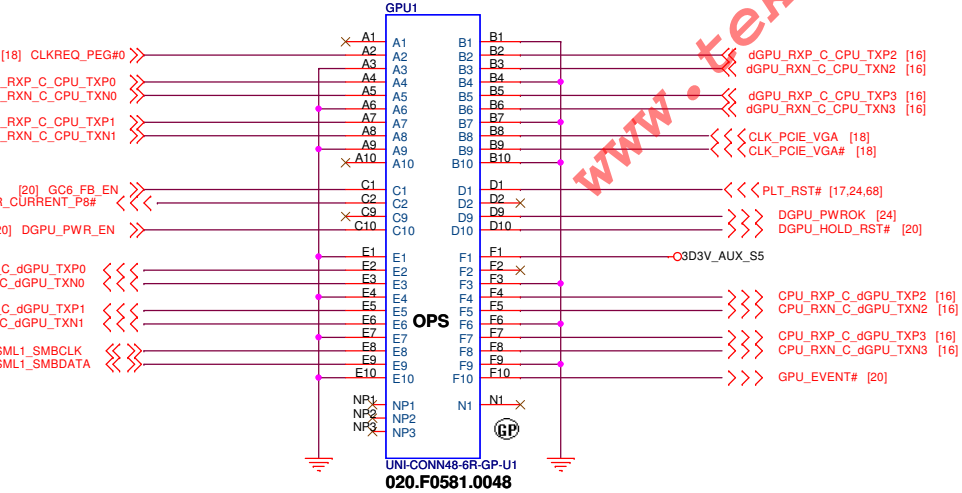
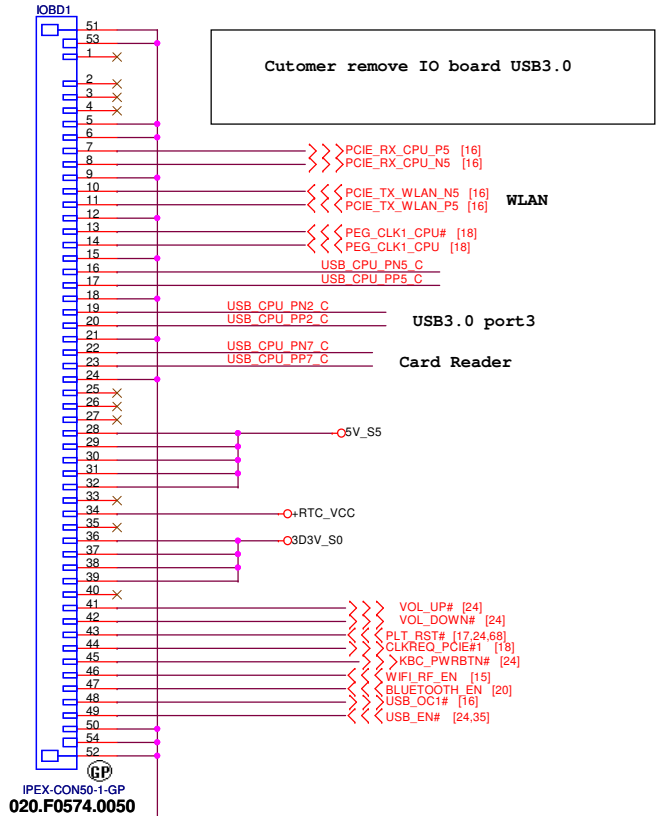
GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)



Main Func = IO Connector



Wistron Confidential document, Anyone can not Duplicate, Modify, Forward or any other purpose application without get Wistron permission

<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **IO Board Connector**


Size A3 Document Number: **Starload SKL-U** Rev: **A00**

Date: Thursday, February 25, 2016 Sheet 66 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

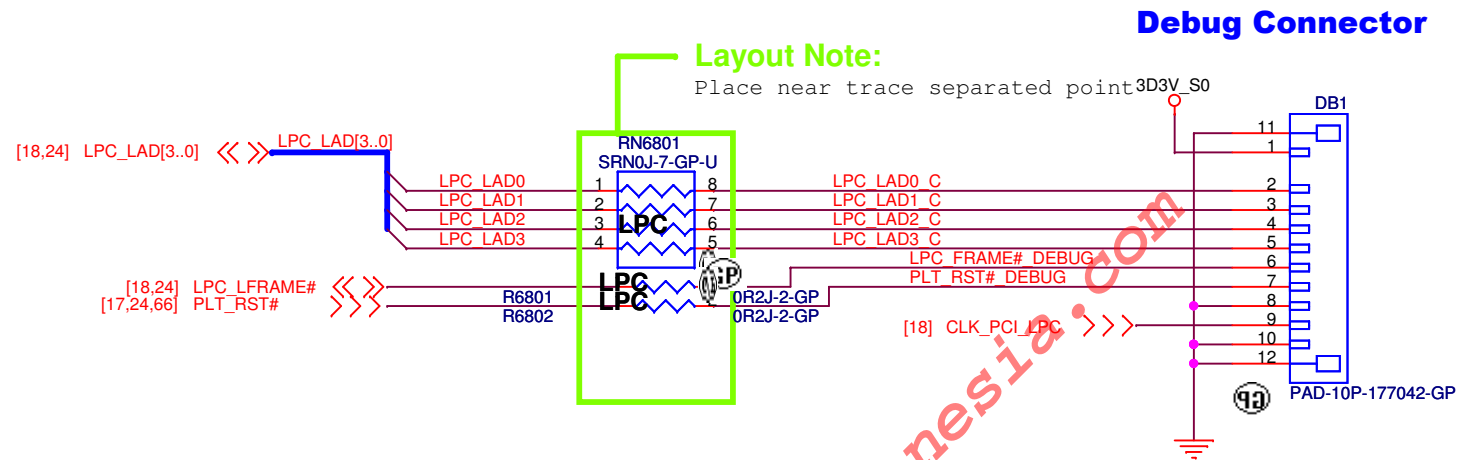
Title

Reserved

Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016	Sheet 67 of 106
-----------------------------------	-----------------

Main Func = Debug



<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Dubug connector

Size
A4

Document Number

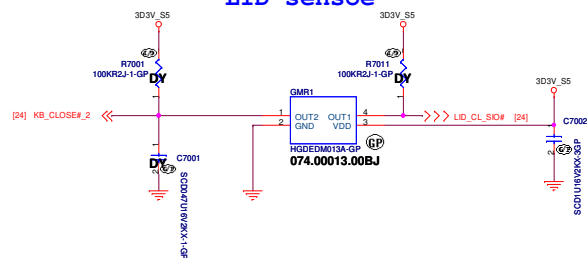
Starload SKL-U

Rev
A00

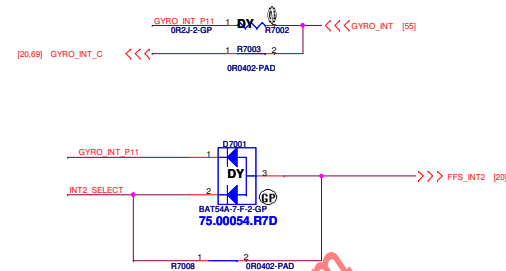
Date: Thursday, February 25, 2016

Sheet 68 of 106

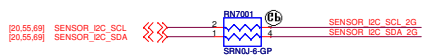
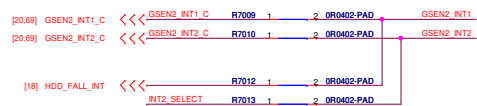
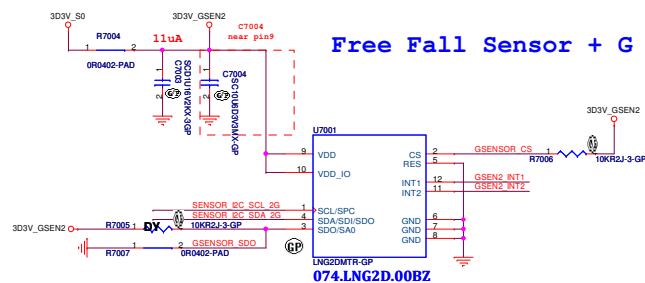
LID sensoe



combine G



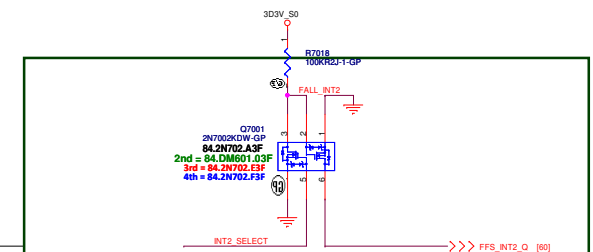
Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Please help to close with U6602



Note:


- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

<Core Design>

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


RESERVED

Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016	Sheet 71 of 106
-----------------------------------	-----------------

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB3.0 PORT


Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016	Sheet 72 of 106
-----------------------------------	-----------------

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved


Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016	Sheet 73 of 106
-----------------------------------	-----------------

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A3

Document Number

Starload SKL-U

Date: Thursday, February 18, 2016

Sheet 74 of 106

Rev


A00

Reserved

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Starload SKL-U

Date: Thursday, February 18, 2016

Rev
A00

Sheet 75 of 106

Reserved

www.teknisi-indonesia.com


www.teknisi-indonesia.com

www.teknisi-indonesia.com

Main Func = dGPU

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU(5/5)PWR/GND

Size

Document Number

Rev

Custom

Starload SKL-U

A00


Date: Thursday, February 18, 2016

Sheet 80 of 106

Main Func = dGPU

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM1,2 (1/4)

Size
A3

Document Number
Starload SKL-U

Rev
A00


Date: Thursday, February 18, 2016

Sheet 81 of 106

Main Func = dGPU

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU-VRAM3,4 (2/4)

Size
A3

Document Number
Starload SKL-U

Rev
A00

Date: Thursday, February 18, 2016

Sheet 82 of 106

Main Func = dGPU

www.teknisi-indonesia.com

Main Func = dGPU

www.teknisi-indonesia.com

```
Main Func = dGFX_CORE
```

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title _____

GPU CORE

Size A2	Document Number Starlead SK1-11	Rev 100
------------	---	-------------------

Date: Thursday, February 18, 2016 Sheet 85 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number
Starload SKL-U

Rev
A00


Date: Thursday, February 18, 2016

Sheet 87 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
Starload SKL-U

Date: Thursday, February 18, 2016

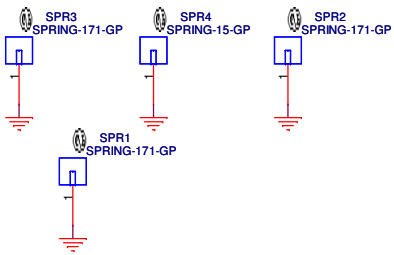
Rev
A00

Sheet 88 of 106

Reserved

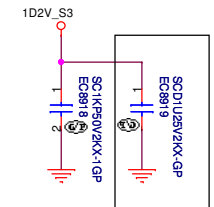
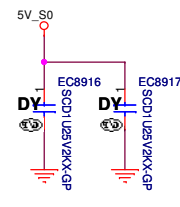
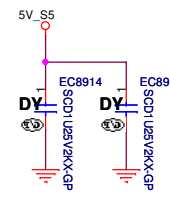
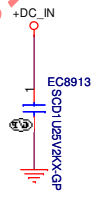
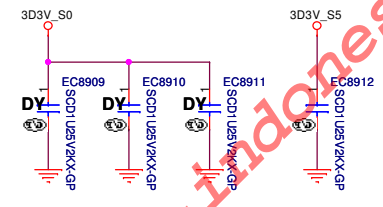
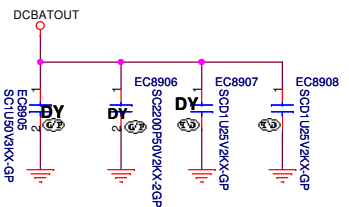
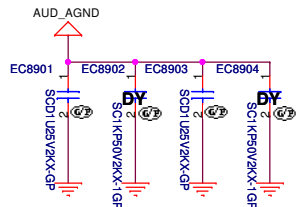
Main Func = UnusedParts

34.4YW18.001



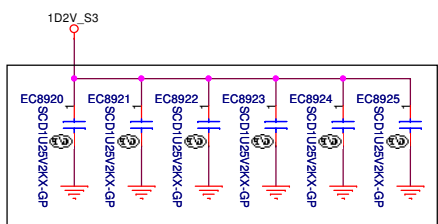
SSID = EMI

Mind the voltage rating of the caps.

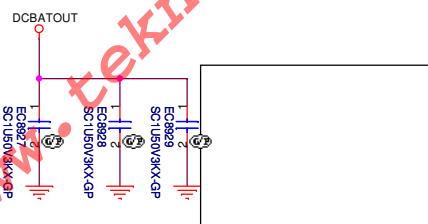


Change to 0.1uF at 20150427 for EMI

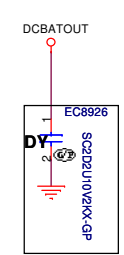
SSID = RF



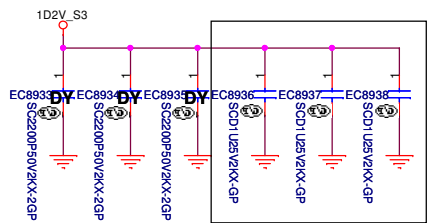
Change to 0.1uF at 20150427 for EMI



Remove EC8931,EC8932,EC8926,EC8930for placement

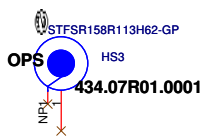
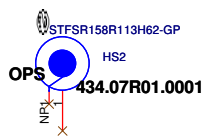
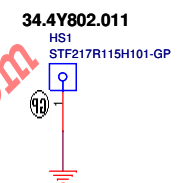
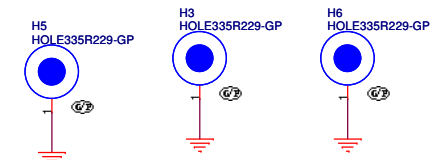


RF request 2016/01/12 modify



Change to 0.1uF at 20150427 for EMI

ZZ.00PAD.7G1



<Core Design>

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: **UNUSED PARTS/EMI Capacitors**

Size A3	Document Number	Rev
Date: Thursday, February 18, 2016	Starload SKL-U	A00
Sheet 89	of 106	

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A3

Document Number

Starload SKL-U

Rev

A00


Date: Thursday, February 18, 2016

Sheet 90 of 106

SSID = TPM

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TPM2.0

Size

A3

Document Number

Starload SKL-U

Rev

A00


Date: Thursday, February 18, 2016

Sheet 91 of 106

(Blanking)

www.teknisi-indonesia.com


<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)Finger Print		
Size A4	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2016		Sheet 92 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)


Size	Document Number	Rev
A3	Starload SKL-U	A00

Date: Thursday, February 18, 2016	Sheet 93 of 106
-----------------------------------	-----------------

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size
A3

Document Number
Starload SKL-U

Rev
A00

Date: Thursday, February 18, 2016

Sheet 94 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size

A3

Document Number

Starload SKL-U

Rev

A00

Date: Thursday, February 18, 2016

Sheet 95 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

(Reserved)

Size
A3

Document Number
Starload SKL-U

Rev
A00


Date: Thursday, February 18, 2016

Sheet 96 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS Switch

Size
A3

Document Number
Starload SKL-U

Rev
A00


Date: Thursday, February 18, 2016

Sheet 97 of 106

(Blanking)

www.teknisi-indonesia.com

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Switch

Size

A3

Document Number

Starload SKL-U

Rev

A00

Date: Thursday, February 18, 2016

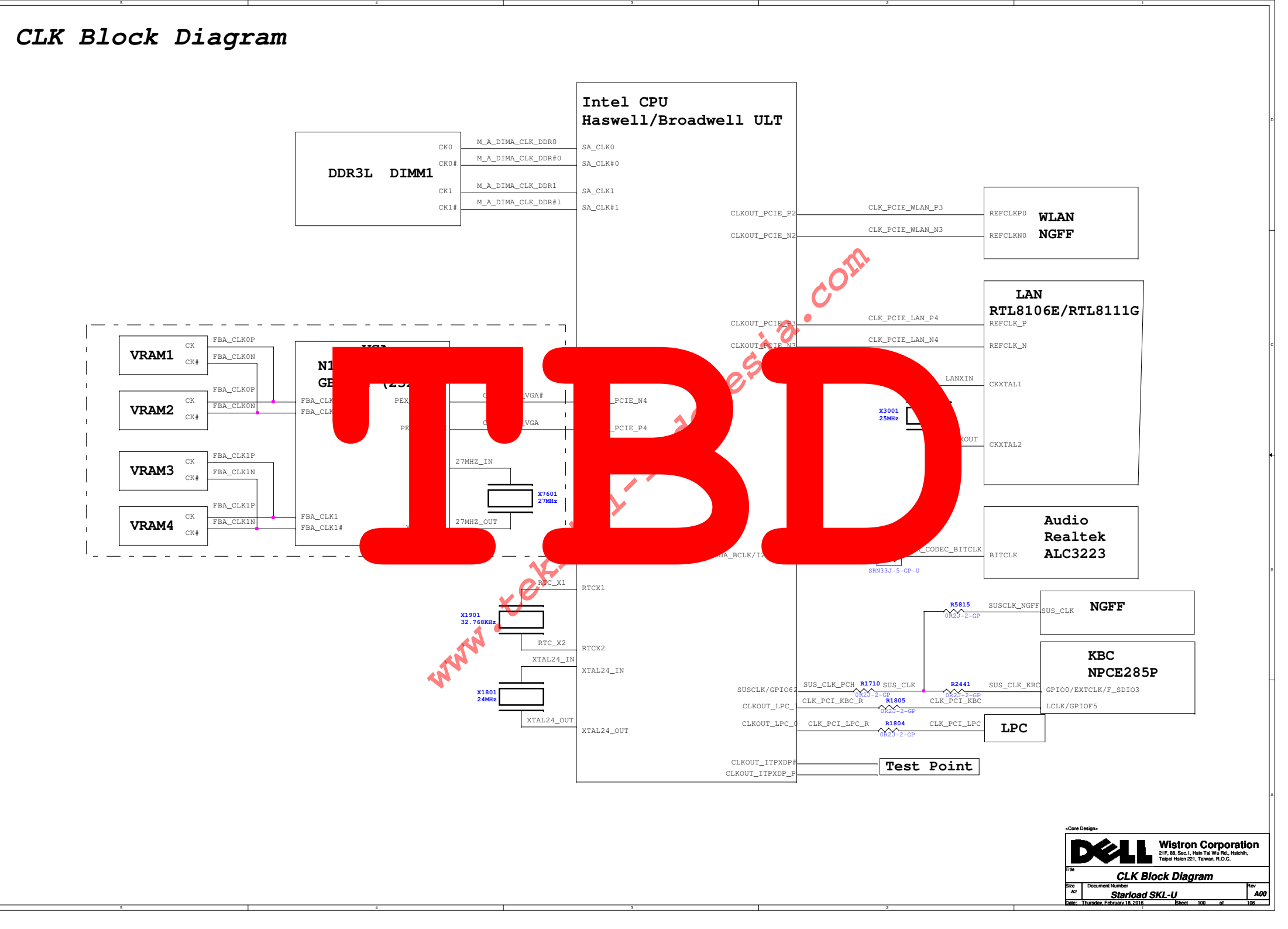
Sheet 98 of 106

www.teknisi-indonesia.com

The diagram illustrates the clock distribution architecture for a Dell Inspiron 15-7000 system. It shows the following components and their clock connections:

- Intel CPU Haswell/Broadwell ULT**: The central processing unit, providing various clock signals like SA_CLK0, SA_CLK#0, SA_CLK1, and SA_CLK#1 to the DDR3L DIMM1.
- DDR3L DIMM1**: Connected to the CPU via M_A_DIMA_CLK_DDR0, M_A_DIMA_CLK_DDR#0, M_A_DIMA_CLK_DDR1, and M_A_DIMA_CLK_DDR#1.
- VRAM1, VRAM2, VRAM3, VRAM4**: Connected to the CPU via FBA_CLKOP, FBA_CLKON, FBA_CLK1P, FBA_CLK1N, FBA_CLK1, and FBA_CLK1#.
- N1 GE**: Connected to the CPU via FBA_CLKOP, FBA_CLKON, FBA_CLK1P, FBA_CLK1N, FBA_CLK1, and FBA_CLK1#.
- LAN (RTL8106E/RTL8111G)**: Connected to the CPU via CLK_PCIE_LAN_P4, CLK_PCIE_LAN_N4, LANXIN, CKXTAL1, and CKXTAL2.
- WLAN (NGFF)**: Connected to the CPU via CLK_PCIE_WLAN_P3, CLK_PCIE_WLAN_N3, REFCLKP0, and REFCLKN0.
- Audio (Realtek ALC3223)**: Connected to the CPU via BITCLK.
- KBC (NPCE285P)**: Connected to the CPU via SUSCLK/GPIO6, CLK_PCIE_KBC_R, CLK_PCIE_KBC, CLK_PCIE_LPC_R, CLK_PCIE_LPC, and CLK_PCIE_LPC.
- LPC**: Connected to the CPU via CLK_PCIE_LPC_R, CLK_PCIE_LPC, and CLK_PCIE_LPC.
- Test Point**: Connected to the CPU via CLKOUT_ITPXPDP# and CLKOUT_ITPXPDP_P.

The diagram also shows various clock signals and their frequencies, such as 27MHz, 32.768KHz, 24MHz, 25MHz, and 27MHz. A large red watermark 'TBD' is overlaid on the diagram.



[illegible]

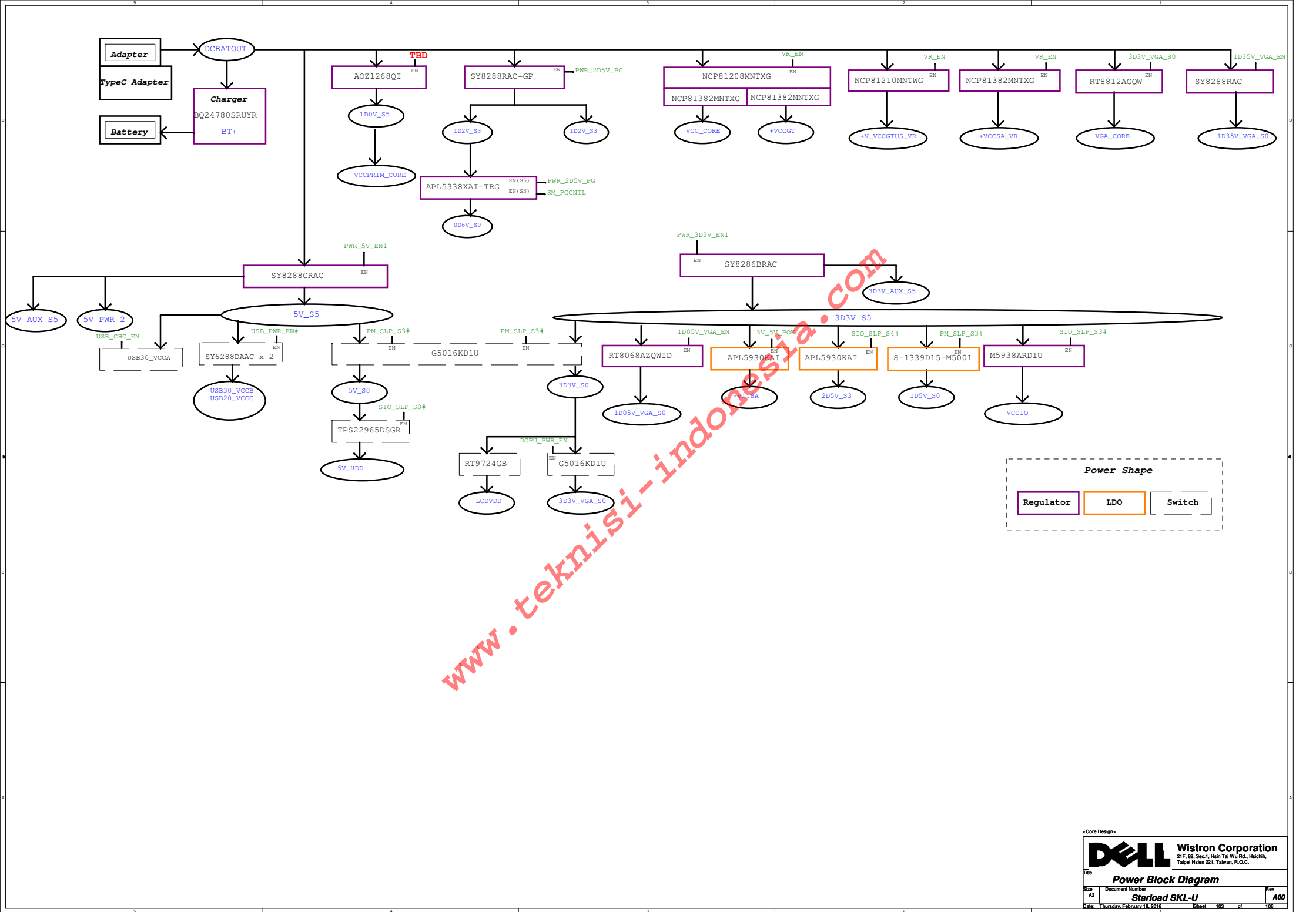
www.teknisi-indonesia.com

There is no specific power down sequence. However, residual voltage from power down must not violate the power-up sequence when back to back GPU power-down and power-up events take place.

- ALL Rail PGOOD#1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During G6x exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/G stays on.
- All delays should be minimized to increase time spent in G6x for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

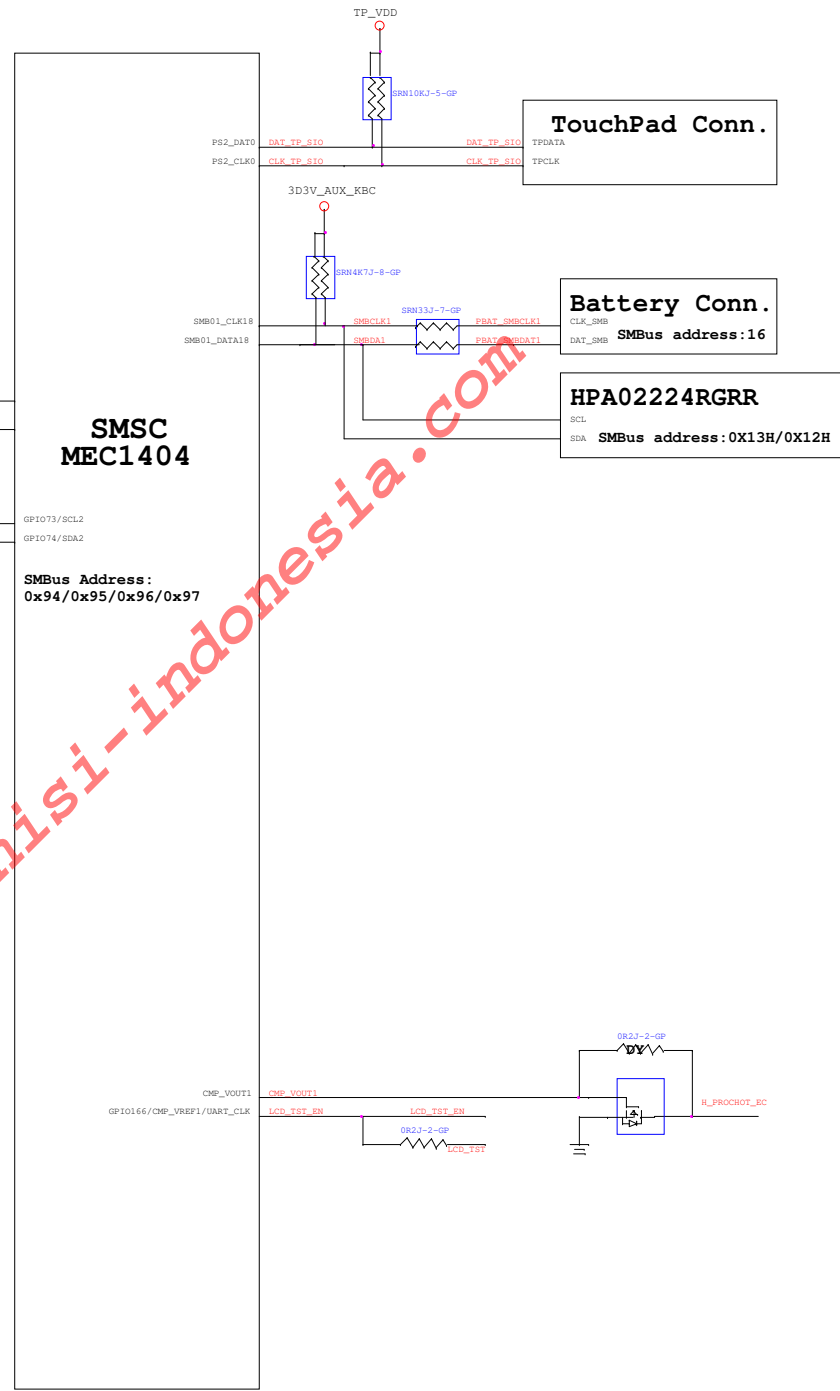
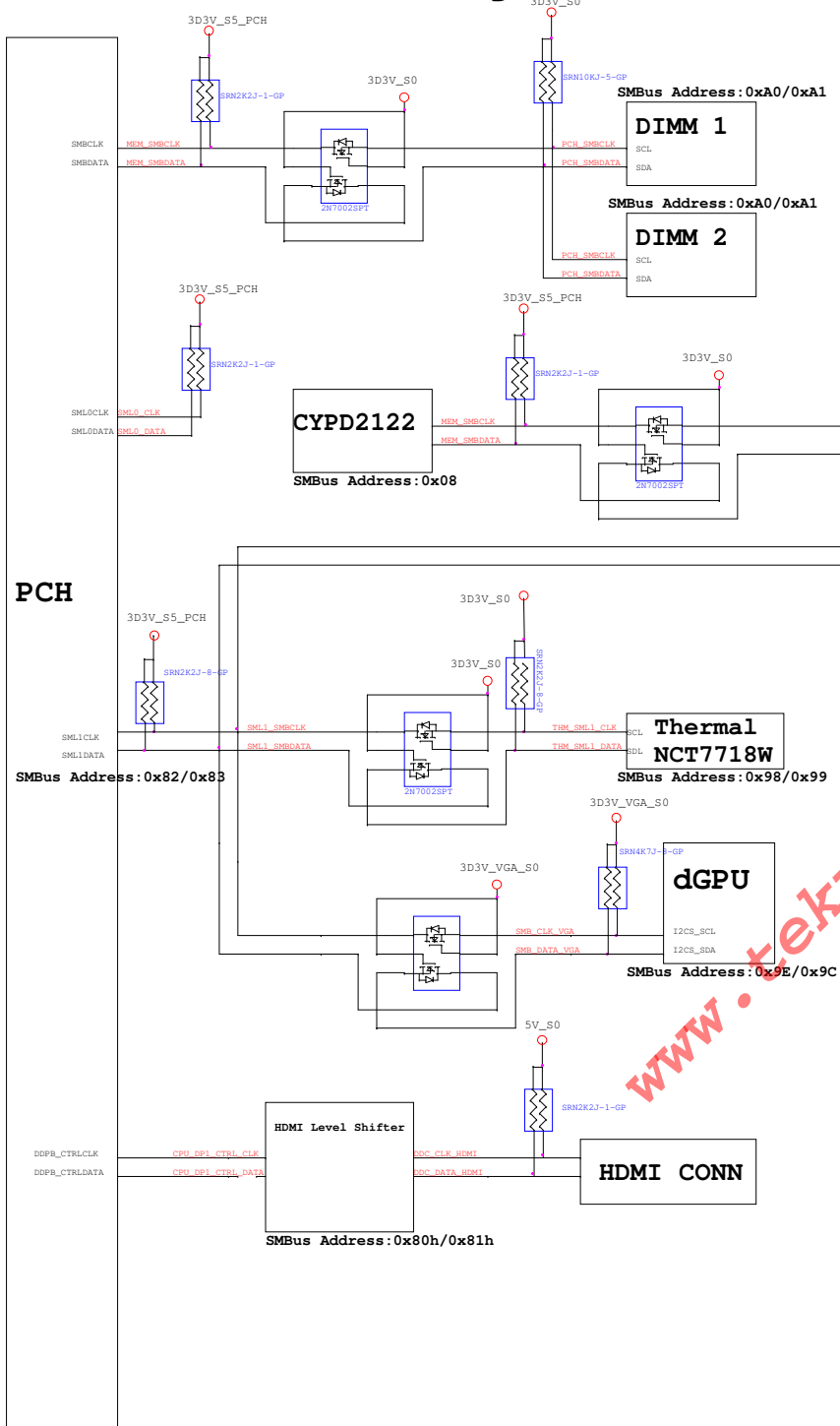
©Case Designs

DELL		Wistron Corporation 207, 2nd, Sec 2, Jhuin Tsp Wd Rd, Hsinchu, Taippei Hsien 300, Taiwan, R.O.C.
Power Sequence		
Standard C81-11		

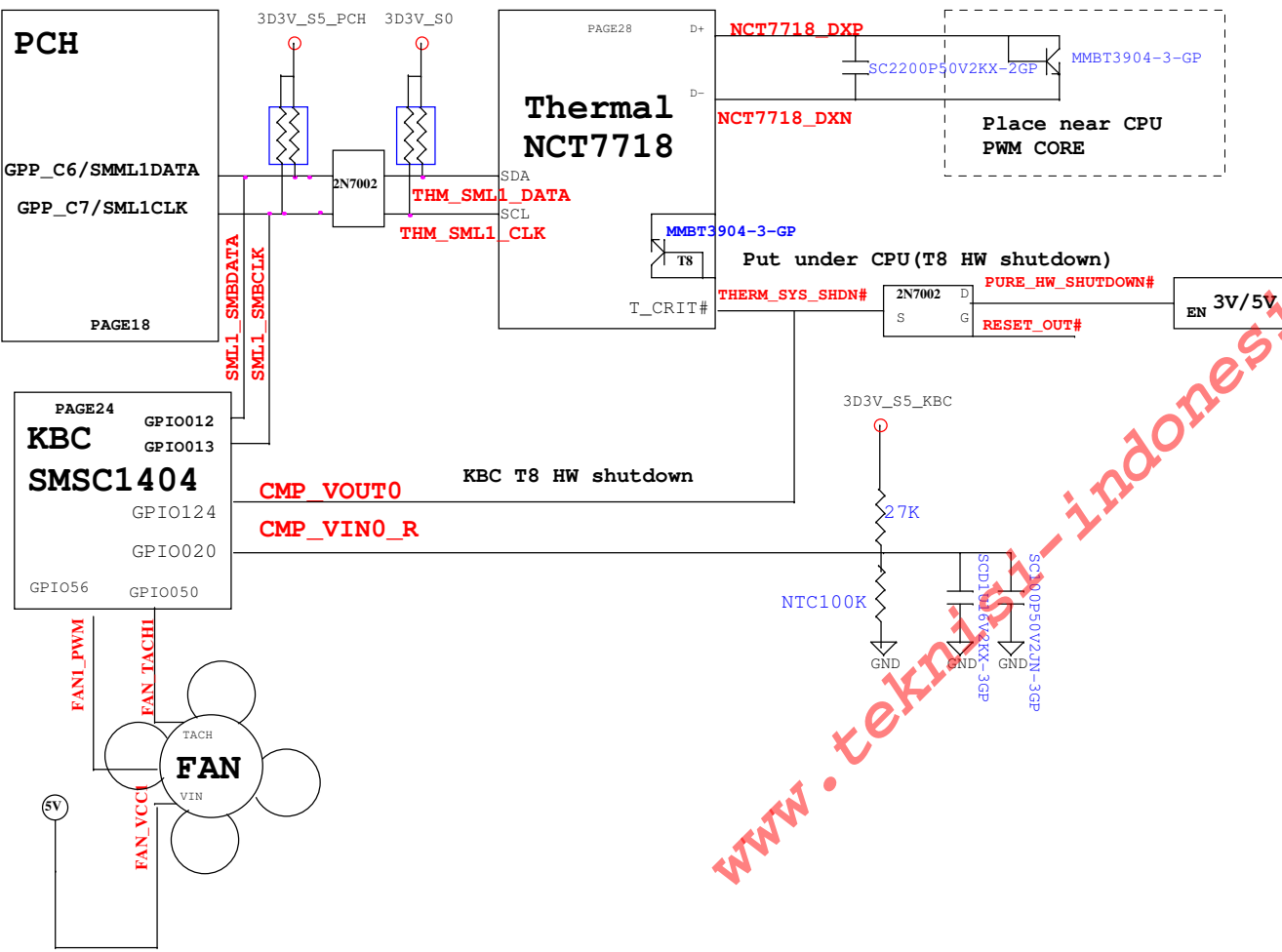


PCH SMBus Block Diagram

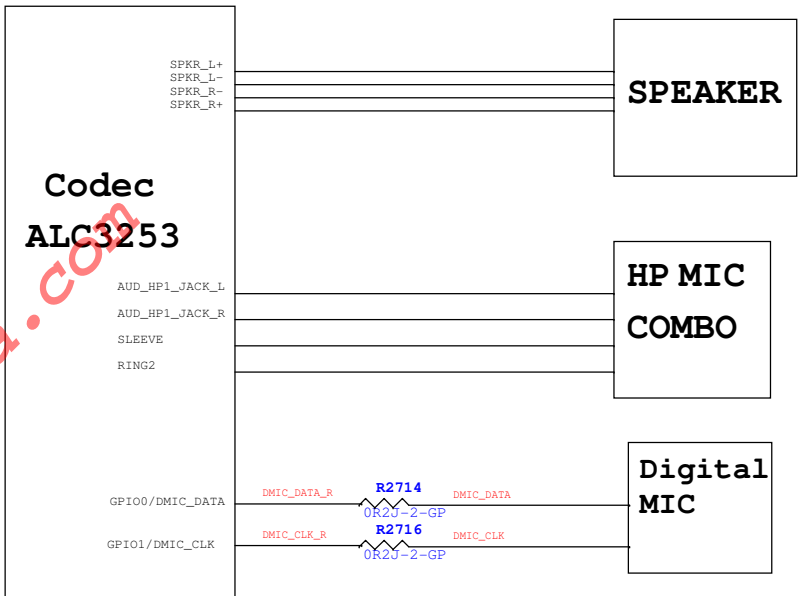
KBC SMBus Block Diagram



Thermal Block Diagram




Audio Block Diagram



www.teknisi-indonesia.com

<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title SIP connector		
Size A	Document Number Starload SKL-U	Rev A00
Date: Thursday, February 18, 2016		Sheet 106 of 106